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MONOLITHIC MICROCIRCUIT
TECHNIQUES AND PROCESSES

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By Bobby W. Kennedy
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June 15, 1972

NASA

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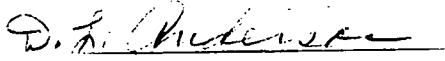
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16. ABSTRACT Contained in this report are brief discussions of the techniques used at MSFC and in industry to make dielectric and metal thin-film depositions for monolithic circuits. Silicon nitride deposition and the properties of silicon nitride films are discussed. Deposition of dichlorosilane and thermally grown silicon dioxide are discussed. The deposition and thermal densification of borosilicate, aluminosilicate, and phosphosilicate glasses are discussed. Metallization for monolithic circuits and the characteristics of thin films are also included.					
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GLOSSARY

ALUMINA - Aluminum oxide (Al_2O_3) pressed in molds and fired produces a ceramic insulator. Alumina is useful as a substrate for hybrid integrated circuits.

ANODIZATION - The formation of an insulating oxide layer on a metal such as aluminum or tantalum by electrolytic action.

CERAMIC - A class of insulating hard materials resembling china or glass, composed of inorganic compounds subjected to heat processing. Used as substrates for film circuits and as packaging materials.

CROSSOVER - A point at which two conductors cross each other. The insulator conductor structure which allows the conductors to cross without shorting.

DIELECTRIC ISOLATION - Most silicon integrated circuits depend on back biased semiconductor junctions to provide isolation between components on the chip. Dielectric isolation involves a number of additional process steps which result in SiO_2 rather than a junction surrounding each component to be isolated. The SiO_2 , a dielectric, provides the necessary isolation.

DIFFUSION - A thermally induced process by which one material may permeate another. In silicon processing, at elevated temperatures doping impurities diffuse into the silicon, forming the desired junctions. These same impurities penetrate SiO_2 much more slowly. Consequently, SiO_2 on the silicon surface serves as a mask to control the areas into which diffusion occurs.

EPITAXIAL LAYER - Semiconductor junctions extend into a silicon surface less than 0.001 inch. Wafers must, however, be several thousandths of an inch thick to avoid excessive breakage in handling but a thick wafer adversely affects component characteristics. The practical solution is to use a heavily doped thick wafer onto which is grown a thin, precisely doped monocrystalline layer of silicon into which the semiconductor junctions are diffused. This layer is called the epitaxial layer. In conventional integrated circuit processing the thick wafer is p doped, the epitaxial layer n doped.

FIELD OXIDE - See Gate Oxide.

GATE OXIDE - For an IGFET gate to be effective in forming a channel beneath it at a low potential, it must be as close to the silicon as possible. Therefore, the oxide under the gate, i.e., gate oxide, is thin. The metal runs between Insulated Gate Field Effect Transistors; however it should not form channels beneath and, therefore, must be made over thicker oxide called the "field oxide."

HERMETIC - Airtight, impervious to external influence, as in an hermetic package. Often used to described metal-to-metal solder or weld-sealed packages. In reality, all materials are permeable, hence specifications define acceptable levels of hermeticity.

HILLOCKS - Small irregularities in the normal surface contour are the result of the stress condition.

METALLIZATION - A metal film selectively deposited on a substrate to serve as conductive interconnections to the elements of the integrated circuit and as points (pads) for external connections.

METAL-NITRIDE-OXIDE SEMICONDUCTOR - Basically an MOS structure to which a Si_3N_4 layer has been added to offset the permeability of SiO_2 by contaminating sodium ions, thus a more stable MOS process. It has also been found that it is possible to generate a relatively nonvolatile memory element by charge storage at the nitride-oxide interface in suitably fabricated devices.

PASSIVATION - The stabilization and protection of component surfaces from environments which might induce changes in characteristics. In monolithic integrated circuits this function is achieved by SiO_2 grown onto the surface of the silicon or by the deposition of glass coating.

QUARTZ - Quartz is crystalline SiO_2 . Thus, the oxidizing of the silicon wafer surface converts it to quartz. The quartz protects the surface of the silicon under it.

SILICON DIOXIDE - The result of oxidizing silicon. Selectively etched SiO_2 permits the selective doping that generates components in monolithic integrated circuits.

SILICON NITRIDE - A silicon compound (Si_3N_4) that is deposited on the surface of silicon monolithic integrated circuits to improve their stability. The nitride is relatively impervious to some ions that penetrate SiO_2 . Best stability is obtained by a combination of Si_3N_4 and SiO_2 . Charge storage at the interface of Si_3N_4 and SiO_2 layer has resulted in memory devices with extremely long retention times.

SILICON OXIDE - A generic term referring to an unspecified mixture of silicon monoxide (SiO) and SiO_2 such as may be deposited on a silicon integrated circuit as an insulator between runs in multilevel metallization.

SPUTTERING - A thin-film technique by which the film material is ejected from the surface of the bulk source by the action of ion bombardment.

THRESHOLD VOLTAGE - Enhancement mode MOS devices require that the gate be forward biased by a threshold voltage before a source to drain channel (and current) develops. This is analogous to the knee in the V_{BE} characteristic of a silicon bipolar transistor.

VACUUM EVAPORATION - A process for generating thin films in which the film material is vaporized and the vapor deposits itself, through openings in a mask, into a substrate.

VIA - Holes or oxide windows for interlayer continuity.

MONOLITHIC MICROCIRCUIT TECHNIQUES AND PROCESSES

SUMMARY

Dielectric and metal thin films are widely used in microelectronics. These films can be deposited by chemical reaction, chemical vapor deposition (CVD), vacuum evaporation, or sputtering techniques. Chemical reaction relies on a chemical reaction between the original surface and its environment. CVD uses either a chemical reaction between two or more substances or a chemical decomposition. Vacuum evaporation occurs when the chamber pressure is reduced to the point where the substance will evaporate. These vapor pressures range from 1 to 10×10^{-3} torr in the temperature range of 600° to 1200° C. Sputtering is a technique in which the material ejected from a bulk source by ion bombardment is used to form the film.

Beam lead chips with silicon nitride passivation offer a tremendous potential for packaging semiconductor circuits. Silicon nitride passivation makes the circuits as failure resistant as conventional circuits in hermetically sealed packages. The silane-ammonia-hydrogen reaction is satisfactory for the deposition of silicon nitride. Ammonia and silane are reacted in the presence of excess hydrogen at about 900° C in an RF-heated horizontal-tube reactor.

Dichlorosilane is an ideal source material for epitaxial silicon film growth. Its low pressure gaseous nature provides convenient delivery to the epitaxial system and low reaction temperatures.

Aluminum oxide may be deposited by the plasma oxidation of aluminum, pyrolysis of aluminum isopropoxide, or the hydrolysis of aluminum chloride. The hydrolysis of aluminum chloride is most used for complementary MOS beam lead devices. The aluminum oxide layers produced by this method have reproducible physical and electrical properties.

CVD processes for synthesizing glass films on semiconductor wafers fall into two basic types: (1) systems based on high temperature (700° to 800° C) reactions using organo-metallic reactants and (2) systems based on low temperature (275° to 475° C) reactions of hydrides and metal alkyls with

oxygen. Glass laminate structures with either graded or abrupt multiple layers can be designed to serve specific purposes in device glassing. Glasses of various properties can be obtained by varying the vapor composition. It is possible, for example, to optimize the thermal expansion of the glass to match a given substrate. Properties of CVD glass films can be substantially improved either by a brief heat treatment at a temperature above that used in deposition, or by a prolonged heat treatment at the temperature of deposition, which can be as low as 450° C. Numerous substrate materials can be glassed. Among these materials are silicon, germanium, gallium arsenide, ferrites, ceramics, and a host of metals. The borosilicate compositions synthesized from diborane, silane, and oxygen at a temperature of 450° C in the rotary reactor apparatus are the most attractive of the binary compositions for device glassing, especially if an over-layer of silicon dioxide is present. They are readily deposited and can be synthesized to closely match the thermal expansion of silicon. Films up to 24- μ m thickness have been deposited on silicon without defect formation. Deposition rates up to 2400 Å per minute have been achieved. The aluminoborosilicate compositions synthesized from trimethyl aluminum, diborane, silane, and oxygen in the rotary reactor have excellent chemical and physical properties. Their composition is more difficult to control than the binary borosilicates and they tend to be less clear. Excellent results have been obtained with lead borosilicate glasses synthesized from tetra ethyl lead, trimethyl borate, tetraethoxy silane, and oxygen in a horizontal tube furnace reactor at 730° C. This process is particularly useful for applications where thin films of high density are required, such as in glassing devices prior to metallization.

One solution to the problems brought about by increasing die size is to use more than one layer of metallization. Two- and three-layer parts can be manufactured reliably with acceptable yields in an aluminum-based system with phosphorosilicate glass passivation. Coverage with both metal and oxide is a prime consideration. Although single-layer parts have some coverage problems, the variety of steps encountered in the multilayer circuit makes the problems more acute.

Important among the factors determining metal coverage is the specific coating system with which metal depositions are made. Even with the most sophisticated designs, the use of increased wafer temperatures and deposition rates appear to be essential to good metal coverage. Step profiling can result in ideal coverage even with nonideal deposition control. Electromigration failures must be compensated for in the design if beveled metallization is employed.

Oxide coverage is important for two reasons. Edge profiles are dependent upon oxide-to-metal thickness ratios and can often be cusped causing almost impossible conditions for metal step coverage. Pinhole protection between two metal layers depends upon how the oxide covers its underlying surface.

I. DIELECTRIC AND METAL FILMS FOR MONOLITHIC CIRCUITS

A. Introduction

The rapid development of the semiconductor industry over the last decade has placed great demands on dielectric and metallization technology since, to a large extent, it controls the technological pace of the electronics industry. This demand has challenged the thin-film technologist to develop new and improved processes for the thin-film conductors and insulation required for semiconductor devices. The variety of materials and processes required to adequately meet the total needs of the industry has necessitated the development of several deposition technologies. Vacuum evaporation, sputtering, chemical vapor deposition, sedimentation, etc., are all in volume manufacturing use and the technologies of each of these techniques have been significantly improved during the past 10 years.

Perhaps the most important reason for the widespread use of thin films in microelectronics is that only thin films can be processed to yield the small size, low power, and high circuit density desired. Thin films are important in other essential processes, e.g., diffusion masking. Also, thin-film deposition techniques allow convenient production of high-purity substances or materials with closely controlled composition. Finally, some vital features of present circuits can be achieved only by using thin films, such as silicon surface passivation with silicon dioxide (SiO_2). Most thin-film applications require either highly conductive or insulating materials, although resistive and semiconductive films have their uses. These films serve as the basis of passive elements, interconnect active elements, protect and insulate various portions of the circuit, connect it to external circuitry, and furnish the active medium of the semiconductor itself. Thin films are used as functional elements of the completed device and are essential in the fabrication of the device.

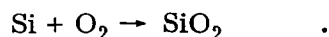
Contained herein are brief descriptions of film deposition methods and the characteristics of various dielectric and metal films. Among the dielectrics described are silicon nitride (Si_3N_4); silicon deposited from dichlorosilane (SiH_2Cl_2), aluminum oxide (Al_2O_3) and Si_3N_4 hermetic seal layers;

thermally grown SiO_2 ; borosilicate, aluminosilicate, phosphosilicate glasses and laminates of these glasses by chemical vapor deposition are also included. Metallization for monolithic circuits includes descriptions of the multilayer metal process, effect of substrate temperature on film deposition and metal sputtering on MOS devices. The characteristics of thin films and beam leaded silicon on sapphire are also discussed.

B. Methods of Film Deposition

Many methods are available for forming surface films and most of them are not recent discoveries. For example, sputtering was observed in the mid-19th century and vacuum evaporation was an annoyance to the early incandescent lamp manufacturers. It will be seen that, within each general type of film deposition method, there is a wide range of materials, properties, and applications. Some of the materials and their applications are shown in Table 1.

1. Chemical Reaction. The chemical reaction between the original surface and its environment can produce a thin layer of a new substance on the surface. The basis of the present technology of silicon devices and integrated circuits in the formation of a thin film of SiO_2 on silicon by the following reaction:



The resulting amorphous SiO_2 layer serves to passivate the surface of the silicon. It also functions as a convenient diffusion mask and provides the electrical insulation between the silicon and the interconnect lines. The SiO_2 layer can be formed in a number of different oxidizing gases, notably steam (H_2O), nitrous oxide (N_2O), and, to a lesser extent, in carbon dioxide (CO_2). Primarily, the reaction is controlled by the rate of diffusion of oxidant across the SiO_2 film, hence, the growth rate decreases with time.

No other common semiconductor forms a naturally occurring oxide film which has useful properties. To a great extent, this is why silicon is predominant in integrated circuit applications.

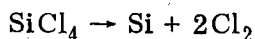
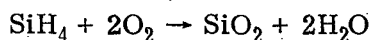
In thermal oxidation, the oxidant diffuses through the growing film to the oxide-silicon interface. There is another class of reactions in which the opposite reaction occurs: The silicon (or conductor) cation migrates toward and reacts with the oxidizing species at the outer surface. It is common to

TABLE 1. THIN-FILM MATERIALS IN MICROELECTRONICS

Purpose						
Interconnections/ Terminals	Insulation/ Passivation	Encapsulation	Resistive	Capacitive	Semiconducting	Processing
Al	SiO ₂ · P ₂ O ₅	SiO ₂	Ta	SiO	Si	SiO ₂
Al alloys (Cu, Si)	SiO ₂	SiO ₂ · P ₂ O ₅	TaN ₂	Ta ₂ O ₅	Se	Si
Cu	Si ₃ N ₄	Al ₂ O ₃	Cr · SiO	HfO ₂	Te	photopolymer
Mo - Au	Al ₂ O ₃	parylene	NiCr	ZrO ₂	SiC	Mo
Ti - Ag	BN	PbO · B ₂ O ₃ · SiO ₂	SnO ₂	PbTiO ₃	GaAs	Cr
Cr - Ag	SiO		kanthal		GaP	
Pt - Au					AlN	
Cr - Cu Au					ZnSe	
Pb - Sn						polymer
						Si ₃ N ₄ - SiO ₂
						PbO
						Nb ₂ O ₅
						Ge - Si - Te
						ZnO

assist the process by making the conductor electrically positive with respect to its surroundings. This is then called anodization and is widely practiced to yield thin oxide dielectric films on metals. It can also be used to produce films on silicon.

2. Chemical Vapor Deposition. Chemical vapor deposition (CVD) employs either a chemical reaction between two or more species or a chemical decomposition to produce the desired film. The latter method is somewhat imprecisely referred to as pyrolysis. In these reactions, the surface does not play an active role in the formation of the thin film. The types of thin films that can be deposited by this method are exemplified by the following reactions:



The third chemical reaction is of particular importance. Depending on the surface conditions and crystal structure, the resulting silicon film can be single crystal or polycrystalline in nature. The former process is called epitaxy and is not usually considered a thin-film process, although most epitaxial silicon films are much less than 5 μm thick and fall within the physical classification of thin films. If the film is polycrystalline, as it is on SiO_2 , then this process is definitely a thin-film process. It is widely used to form the gate electrode in the silicon self-aligned gate FET process.

A practical CVD process requires a suitable compound to carry the desired substances to the surface, a heterogeneous gas-solid reaction whose rate is much faster than any competing process and a reactor system which assures temperature uniformity, gas composition homogeneity, and a reasonable batch size. Temperature control is important since the reaction is usually thermally activated. However, the substrate temperatures needed for film deposition may be lowered appreciably by supplying RF or microwave energy to create a plasma or glow discharge. Films of SiO_2 and Si_3N_4 are often deposited in this way but reproducible film properties are sometimes difficult to achieve.

The deposition of SiO_2 is one of the most widely used CVD processes. In addition to pure SiO_2 , processes have been developed to incorporate stabilizing substances into the basic SiO_2 matrix; glassy materials containing

phosphorus, aluminum, boron, etc., have been deposited as thin films. In addition to polycrystalline silicon, a number of thin metal films can be formed by CVD. Both molybdenum and tungsten can be deposited by decomposing their halides or carbonyl compounds.

3. Vacuum Evaporation and Sputtering. If the pressure inside a chamber is reduced sufficiently, substances will evaporate. Their atoms or molecules will travel in straight trajectories if the pressure is so low that their mean free path is of the same magnitude as the dimensions of the chamber. This is the basic principle of vacuum evaporation. A substance must attain a vapor pressure of $\sim 10^{-2}$ torr to deposit at a useful rate. For most materials, this means that an elevated source temperature is necessary. The rate of film growth depends on the rate of arrival of evaporant particles and the probability of a given particle being retained on the surface. The latter is measured by a parameter called the sticking coefficient. Some important factors in vacuum evaporation are the vacuum required, the nucleation of the initial deposit, and the stability of the evaporating substance. The most successful substances for thin film formation are elements or simple compounds whose vapor pressures range from 1 to 10×10^{-3} torr in the temperature interval 600° to 1200°C . The level and composition of background gases are important if the film properties are sensitive to impurity atoms.

A great deal of investigation has gone into appropriate means of maintaining the source of evaporating material at the desired temperature. The earliest sources were refractory metals such as tungsten which could be heated by passage of a dc current. Later, boats of various materials such as molybdenum, graphite, and boron nitride (BN) were developed. In addition to direct electrical heating, inductive methods are also used. By using RF induction and large diameter inert crucibles, evaporation of a number of different metals at high rates in a single evaporator cycle is possible. The major problems with this method are the probability of contamination of the deposit by the source and source failure.

To circumvent these problems, a focused electron beam can be used to heat a portion of the material. While minimizing contamination and allowing significantly higher temperatures to be attained so that more refractory substances can be evaporated, electron beam evaporation is more costly and complex. The X-radiation from the source may be a factor in certain applications such as MOSFET device threshold voltages.

Another method which has found increasing use is the deposition of a liquid suspension of appropriate materials followed by conversion to a glass-like film from which diffusants can be supplied to the semiconductor. These

are often referred to as doped-oxide or paint-on sources. The technique combines the ease of pattern formation with the advantages of the planar diffusion process. Some available diffusants are phosphorus, boron, arsenic, and gold. One difficulty with this technique is the inability to get a reproducible high surface concentration of diffusant. Another is the susceptibility to deleterious ionic contamination.

II. DIELECTRIC SUBSURFACE INSULATOR LAYER FOR MONOLITHIC CIRCUITS

A. Silicon Nitride Systems

1. Introduction. Si_3N_4 passivation offers tremendous potential for packaging semiconductor circuits. A surface of Si_3N_4 passivation, for example, makes them as failure-resistant as conventional circuits in hermetically sealed packages. While most of the methods for the synthesis of Si_3N_4 are particularly applicable to large ceramic objects, some of them (e.g., the silane (SiH_4), ammonia (NH_3), hydrogen (H_2) reaction described herein) are satisfactory for thin film deposition. The flow system for Si_3N_4 deposition can be of the conventional type and the reactor can be a resistance-heated horizontal cold wall unit. The substrates used for film deposition can be single crystal silicon of various orientations. Vapor phase etching (e.g., hydrogen chloride (HCl) in H_2 at 1200°C) can be used for substrate cleanup prior to these depositions. Omission of this step usually produces films with many visible defects, but it has been reported that, if the film is to be used as the insulator in an MOS transistor, etching is deleterious.

2. Morphology and Film Composition. Films deposited at temperatures below 900°C appear amorphous and show no X-ray diffraction lines. Between 900° and 1000°C some small crystallites grow over the surface, and above 1100°C they are almost continuous. Figure 1 shows representative areas from each of these temperature ranges. Others have not reported the high crystallite concentrations at temperatures as low as 1100°C . Emissivity correction of the temperature combined with higher deposition and flow rates which have been used could explain the difference. X-ray diffraction data indicate that these crystallites are α Si_3N_4 .

Composition of the amorphous films has not been determined. There are some data based on activation analysis which indicate a possible neutron of Si (HN_2)₄. Direct chemical analysis of films prepared in similar fashion indicated a composition of Si_3N_4 . Because of the varying physical properties

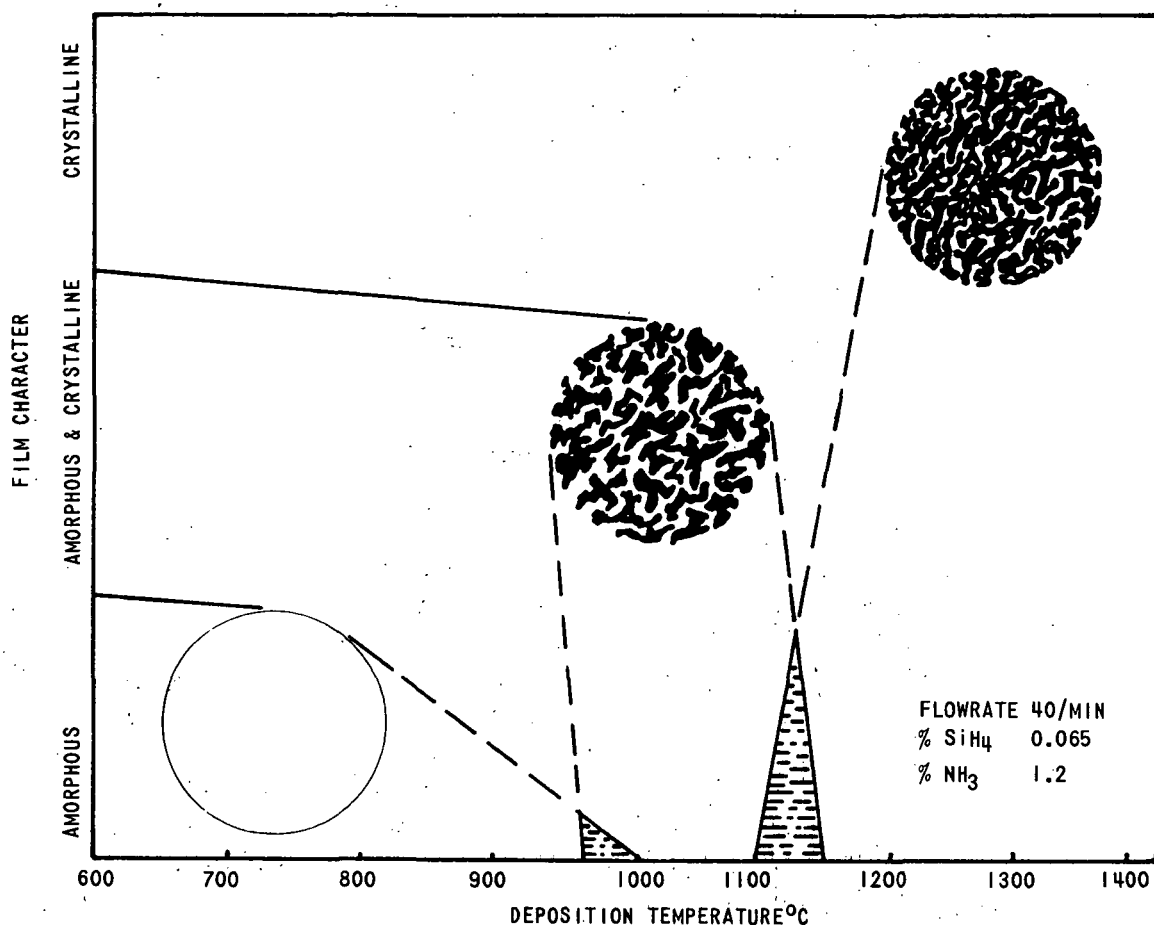


Figure 1. Film character versus deposition temperature.

that have been observed as deposition conditions are changed, it is probable that the actual amorphous film composition can be varied over rather wide limits from silicon rich to nitrogen rich. Additionally, films deposited at lower temperatures may contain hydrogen as well as silicon and nitrogen.

3. Deposition Behavior. The effect of temperature on deposition rate is shown in Figure 2. Log rate versus $1/T$ plots are given for the concentrations of 0.095 and 0.065 percent SiH_4 (all percentages are volume percent) with a fixed concentration of 1.2 percent NH_3 . The film growth rate increased rapidly with temperature up to about 900°C . Above this temperature the growth rate becomes less temperature dependent.

There are three possible explanations for the apparent change in deposition rate:

a. The basic problem with SiH_4 is that it starts the decomposition before it reaches the substrate.

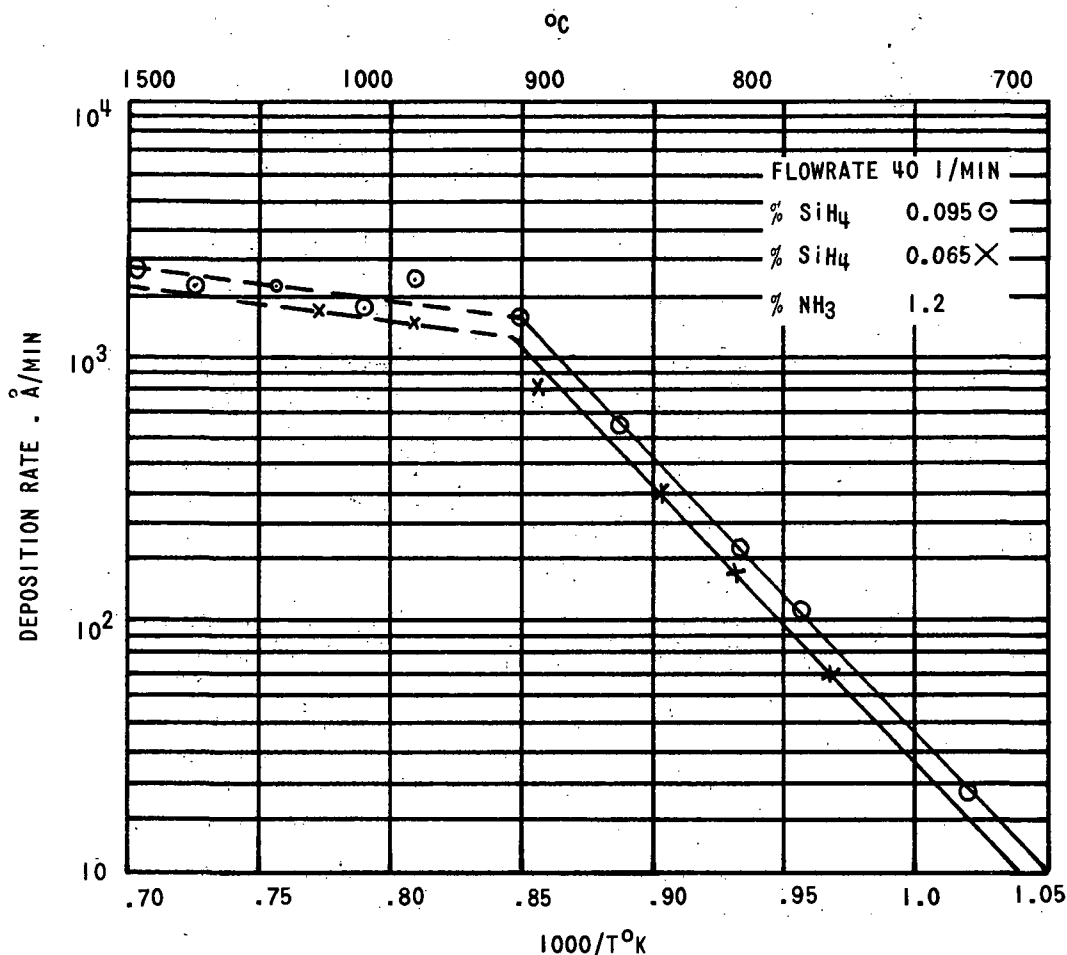


Figure 2. Deposition rate versus temperature.

b. The difficulty of measuring film thickness by ellipsometer when crystallites start to cover the surface. The energy striking the surface is scattered, and only a portion is returned to the ellipsometer detector.

c. The decrease may mark the entrance into a diffusion controlled reaction which would be expected to be nearly temperature insensitive.

A plot of deposition rate as a function of percent SiH₄ at deposition temperatures of 850 and 875° C is shown in Figure 3. These data indicate a linear relationship of deposition rate with respect to SiH₄ concentration. Extrapolation of the curves indicate a deposition rate approaching zero at 0 percent as would be expected.

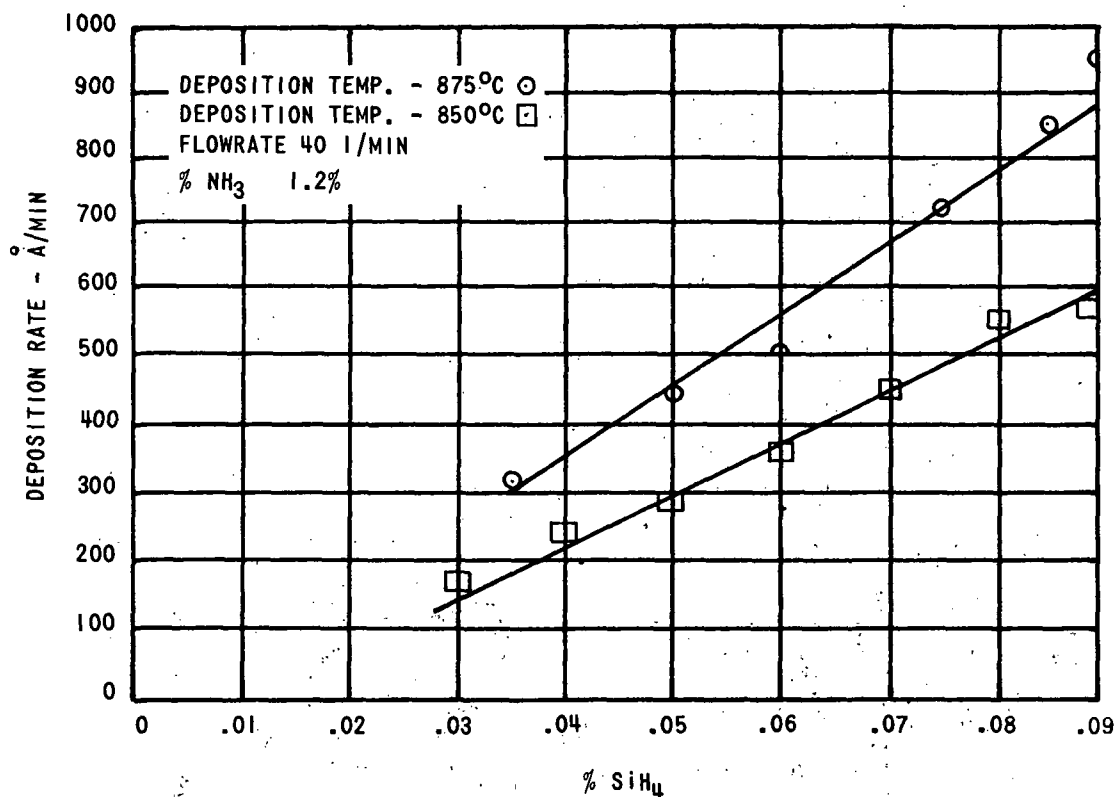


Figure 3. Deposition rate versus percent SiH₄.

Plots of deposition rates as the function of NH₃ in concentrations of 0.03, 0.065, and 0.095 percent SiH₄ are shown in Figure 4. Below an NH₃ concentration of about 0.3 percent there is an increase in deposition rate due apparently to a change in the stoichiometry of the film. It is postulated that films deposited with an NH₃ concentration below 0.3 percent and with a 0.065 percent SiH₄ concentration are silicon rich. This corresponds to a SiH₄ - NH₃ ratio of approximately 1:5. For the other two SiH₄ percentages shown, the increase in deposition rate occurs at nearly the same SiH₄ - NH₃ ratio. It is also interesting to note that the deposition rate at very low NH₃ concentration approaches the silicon deposition rate from pure SiH₄ in the reactor.

4. Etching. Etch rates have been determined using Bell No. 2 etch contained in a constant temperature bath which was controlled to within $\pm 0.1^\circ \text{C}$ of the desired temperature. Slices with known Si₃N₄ film thickness have been etched for a specified length of time with constant stirring and then remeasured on an ellipsometer to determine the change in film thickness. The effect of etch temperature on etch rate is shown in Figure 5. The films were deposited at the usual deposition conditions. Calculation of apparent activation energy from these data gave a value of 15 kcal/mole.

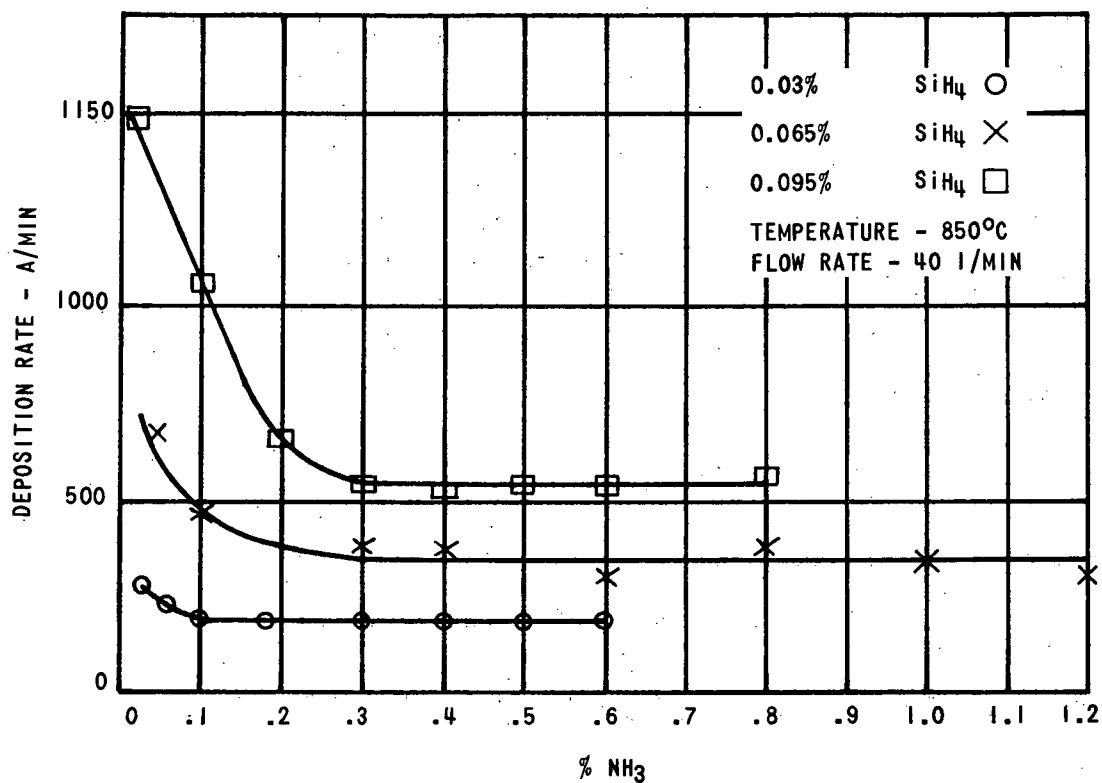


Figure 4. Deposition rate versus percent NH_3 .

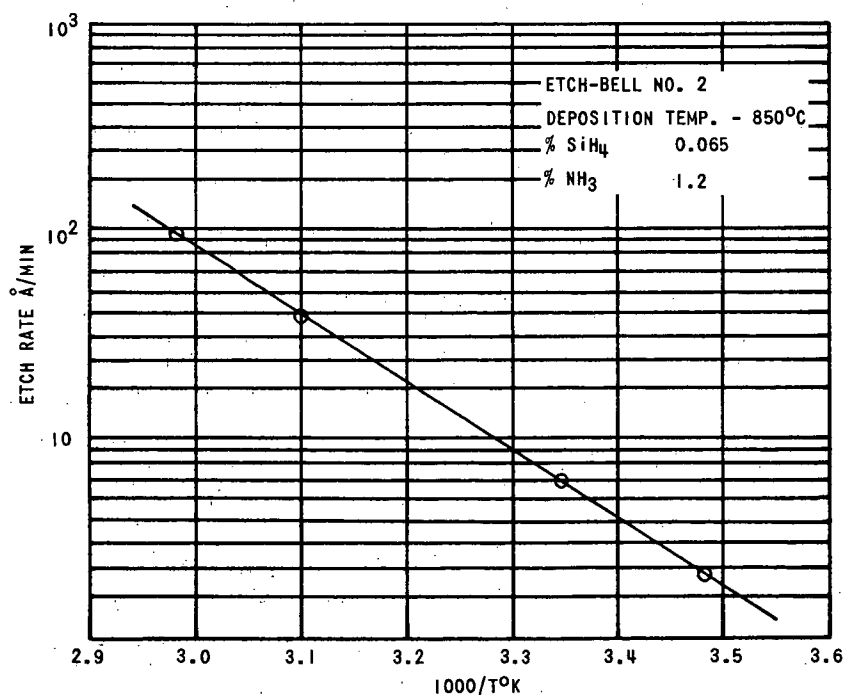


Figure 5. Etch rate versus etchant temperature.

A plot of etch rate versus changing NH_3 concentration at an etch temperature of 25°C is shown in Figure 6. Above approximately 0.4 percent NH_3 , the etch rate is uniform ($\sim 6.25 \text{ \AA}/\text{min}$), but below this concentration the etch rate decreases rapidly and approaches zero. This is taken as additional evidence that the films become silicon rich in this region and with Bell No. 2 as an etchant this increase in etch rate is expected. The effects of varying the SiH_4 percentage on the etch rate can be seen in Figure 7. Again, as the films become silicon rich, the etch rate decreases.

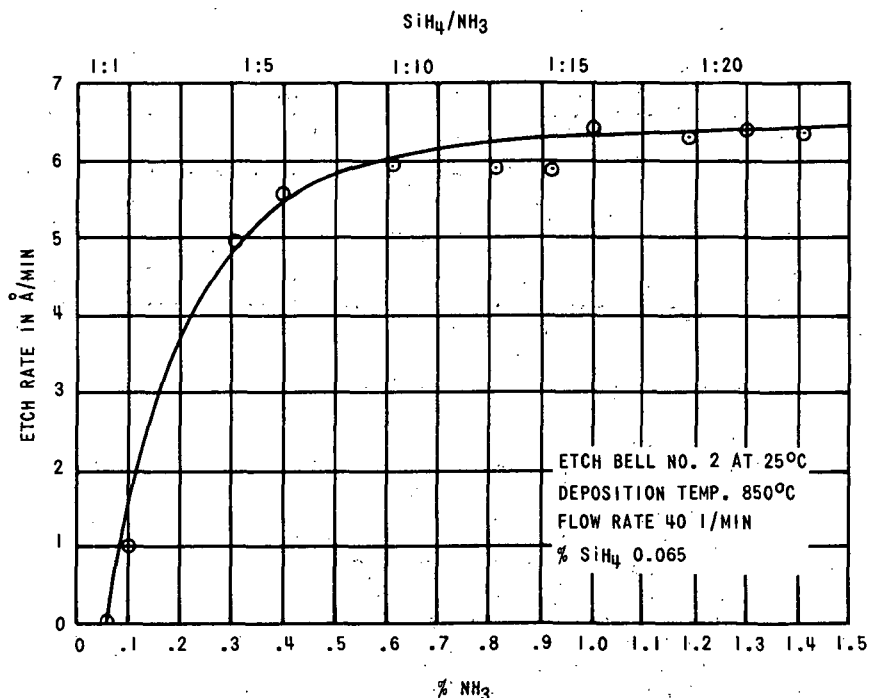


Figure 6. Etch rate versus percent NH_3 .

The etch resistances of $2000\text{-}\text{\AA}$ Si_3N_4 and thermally grown SiO_2 films to a mixture of 5 percent HCl in H_2 at 1200°C for 2 minutes were compared. The Si_3N_4 film was impervious while the SiO_2 film was completely removed and etching of the silicon surface occurred.

5. Optical Properties. Optical transmittance data were obtained over the range from 0.2 to $24 \mu\text{m}$. Between 0.2 and $0.4 \mu\text{m}$, films deposited on fused silica blanks were used. Between 0.4 and $8 \mu\text{m}$ there appear to be no absorption bands. Above $8 \mu\text{m}$ the most prominent absorption is that due to the silicon-nitrogen which occurs in the 10 to $12 \mu\text{m}$ range as shown in Figure 8.

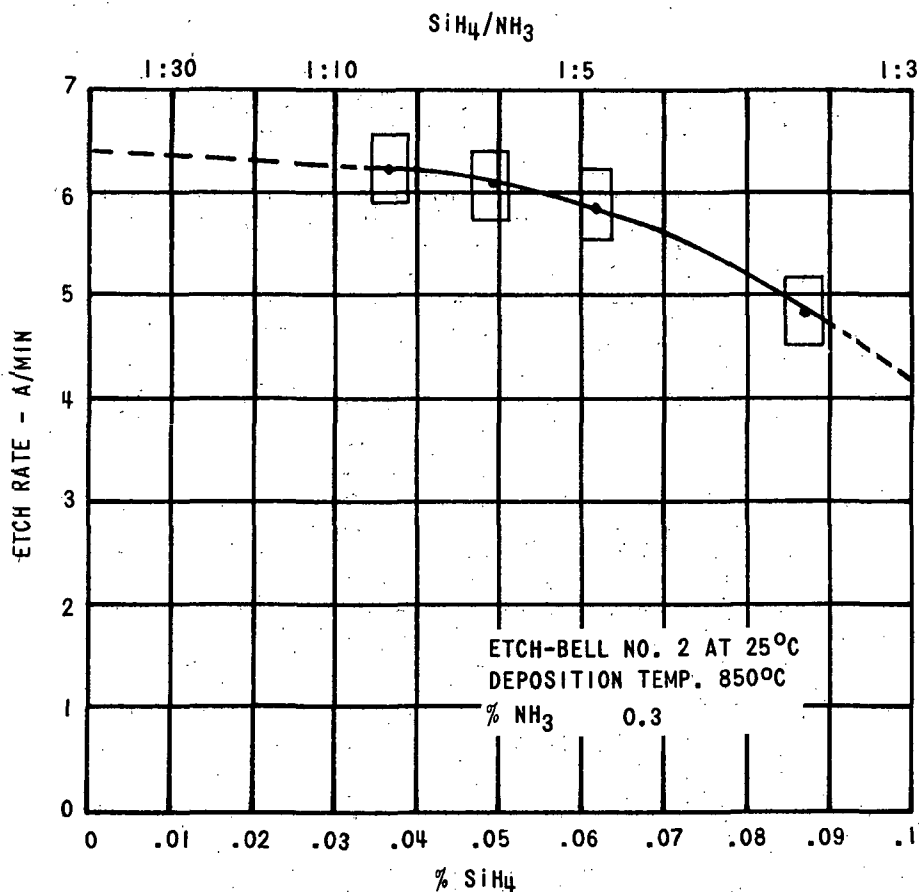


Figure 7. Etch rate versus percent SiH₄.

The index of refraction of several films was determined from ellipsometer measurements at 5461 Å. In Figure 9 the refractive index versus NH₃ percentage is shown for 0.065 percent SiN₄. Over most of the composition range, it varied from 2.0 to 2.05, but, as the gas stream percentage of NH₃ decreased below 0.3 percent, an increase in the index of refraction occurred. The index increases uniformly to that of silicon (about 4.02) as the NH₃ concentration is decreased to zero. This is taken as confirming evidence of the silicon rich nature of each film.

6. Deposition of Silicon Nitride Using RF Epitaxial Reactor. Si₃N₄ as a hermetic-seal layer is well known and can be deposited using an RF heated horizontal or vertical reactor in much the same way as discussed above using a cold wall resistance heated tube.

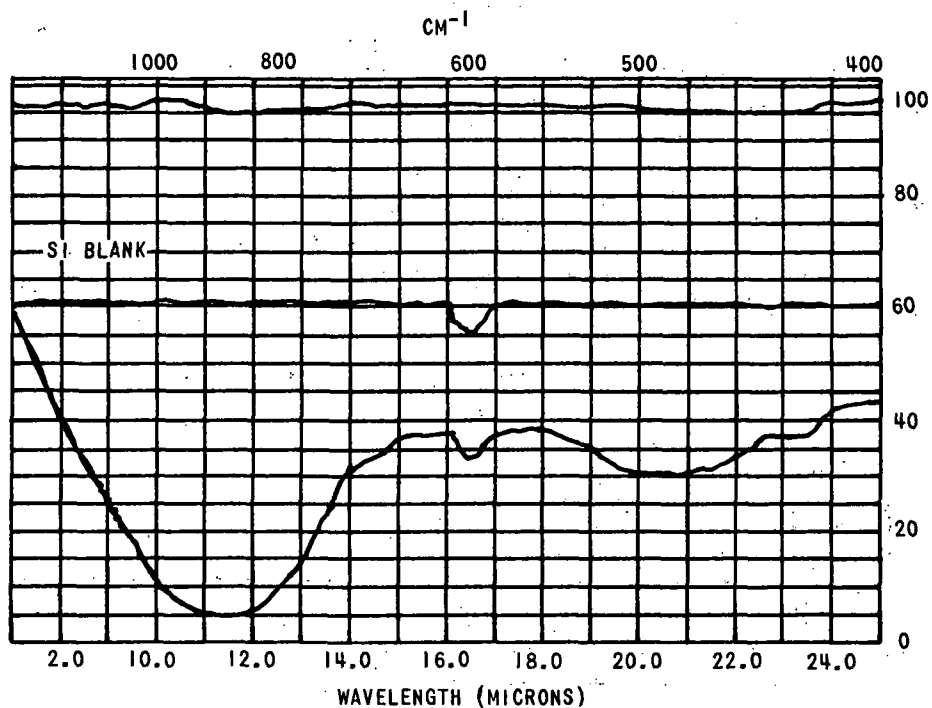


Figure 8. Infrared transmission (8.0 to 24 μm) to silicon nitride.

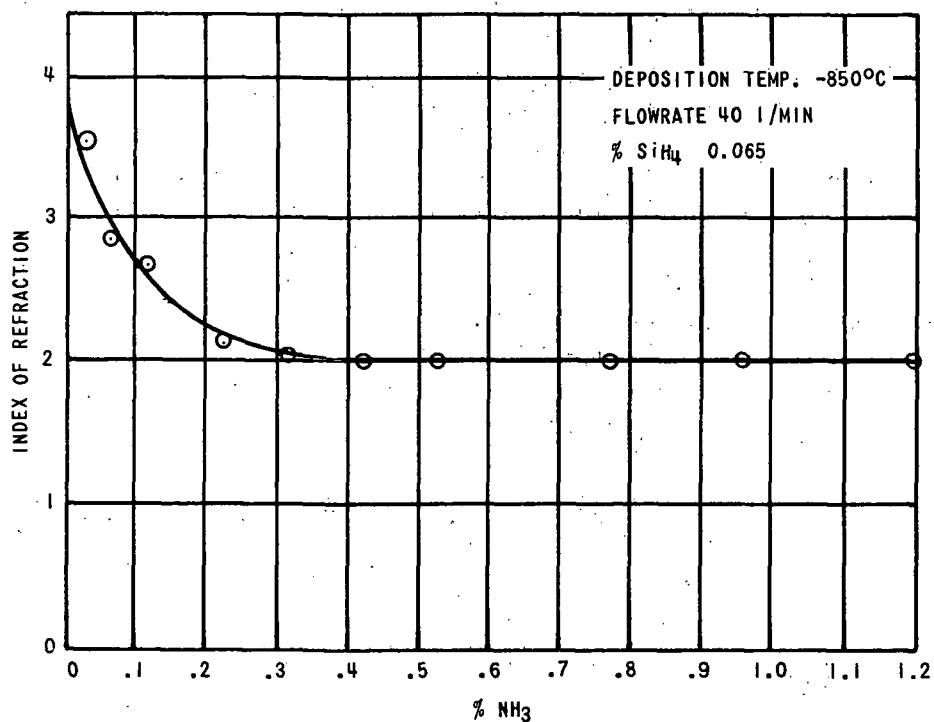
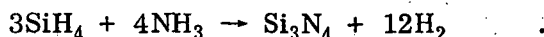


Figure 9. Index of refraction versus percent NH_3 .

Deposition of Si_3N_4 is accomplished by reacting NH_3 and SiH_4 in the presence of excess H_2 . A simple expression for the reaction, which is carried out about 900°C , is



The apparatus used for depositing Si_3N_4 films is shown in Figure 10. It consists of an RF-heated horizontal-tube reactor similar to equipment used for the epitaxial deposition of silicon. The wafers are carried on a graphite block susceptor that is coated with silicon carbide (SiC). The reactant gases — SiH_4 [3 percent SiH_4 in nitrogen (N_2)], NH_3 , and forming gas (to supply the excess H_2) — are piped into the system through metering valves, flow-meters, and filters.

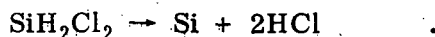
The effects of process variables on the growth rate and properties of insulating films grown from an H_2 - SiH_4 - NH_3 mixture are well known. Growth rate versus $1/T$ has a break at 900°C which coincides with an amorphous-polycrystalline transition. Hardness, growth rate, and refractive index move toward values appropriate for silicon as the percent NH_3 is reduced. The thermal expansion coefficient can be varied from approximately that of silicon to appreciably more by increasing the percent NH_3 .

The best quality of Si_3N_4 films for application to complementary MOS integrated circuits thus far, however, has been obtained from the RF-heated system.

B. Deposition of Dichlorosilane

Dichlorosilane (SiH_2Cl_2) has many attributes which make it an ideal source material for epitaxial silicon film growth. Its low pressure gaseous nature provides convenient delivery to the epitaxial system. Thermodynamic analysis of the SiH_2Cl_2 - H_2 system indicates high conversion to silicon and low reaction temperatures.

SiH_2Cl_2 occupies an intermediate position in the monosilane (SiH_4)-silicon tetrachloride (SiCl_4) series. Its principal high temperature reaction, similar to SiH_4 , is one of simple pyrolysis:



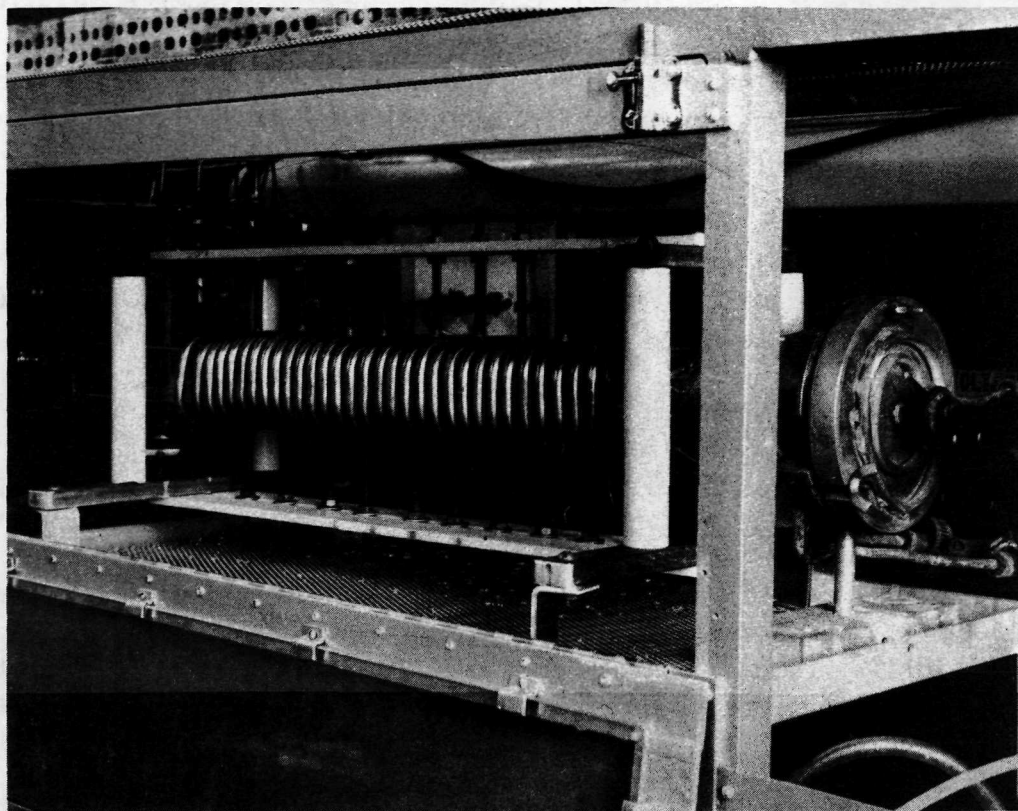
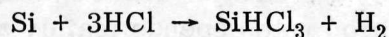


Figure 10. RF-heated silicon nitride deposition system.

In contrast to SiH_4 , however, the formation of HCl as a byproduct leads to a series of reverse reactions:



Processing in excess H_2 tends to suppress these reverse reactions and the further conversion of SiCl_2 into higher SiH_4 polymers. Under typical silicon epitaxial processing conditions in a H_2 carrier, conversion of SiH_2Cl_2 to silicon is high, with HCl , SiHCl_3 , and unreacted SiH_2Cl_2 the principal byproducts.

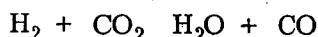
SiH_2Cl_2 provides significant advantages for the growth of epitaxial silicon films. The temperature coefficient of growth rate is very small. The

temperature of effective epitaxy is low, i.e., 1050° to 1100° C (optional). The rate of the surface reaction is rapid and high rates of film growth of excellent quality are readily achieved. The rate of film growth is independent of doping level. The operational characteristics of SiH_2Cl_2 are similar to SiCl_4 . SiH_2Cl_2 may be used in current epitaxial systems without system modification.

C. Hermetic-Seal Layer (Aluminum Oxide and Silicon Nitride)

It has been found that a sandwich insulator, using a layer of SiO_2 and either Si_3N_4 or aluminum oxide (Al_2O_3), can be used for complementary MOS integrated circuits. Because of the higher dielectric constant of Si_3N_4 or Al_2O_3 , thicker gate insulators can be used for a given gate capacitance, providing higher gate-breakdown voltage, reducing pinhole problems, and enhancing reliability. Although both Al_2O_3 and Si_3N_4 are suitable for application to complementary MOS circuits, each material offers some different advantages.

High-quality Al_2O_3 layers may be deposited by either plasma oxidation of aluminum, pyrolysis of aluminum isopropoxide [$\text{Al}(\text{OC}_3\text{H}_7)_3$], or hydrolysis of AlCl_3 . The hydrolysis of AlCl_3 is the most used process in industry to deposit the hermetic layer in complementary MOS beam-lead devices. In this technique, AlCl_3 (a solid at room temperature) is reacted with water generated by the reaction of H_2 and carbon dioxide (CO_2) at about 900° C:



H_2 is used both as the ambient gas and as the carrier gas and it greatly exceeds the concentration of both CO_2 and AlCl_3 . The CO_2 concentration exceeds that of the AlCl_3 , so the deposition rate depends mainly on the AlCl_3 concentration. The amount of water vapor is proportional to the concentration of CO_2 and water vapor is formed only when the H_2 and CO_2 are in contact with the heated wafer. The water then reacts locally with the AlCl_3 vapor.

Solid AlCl_3 is kept in a leakproof stainless-steel chamber that has one inlet and one outlet. The chamber is kept in a constant-temperature oven. The oven temperature determines the partial pressure of the AlCl_3 and, therefore, its concentration in the carrier gas. H_2 is passed over the AlCl_3 , and the passage is baffled so that saturation of the carrier gas is ensured.

Upon emerging from the outlet, the gas stream is mixed with H_2 and CO_2 and is passed into the reactor chamber.

There are several round SiC coated carbon susceptors in the growth chamber, each holding a silicon wafer. The susceptors are positioned on quartz tracks and in quartz rotation assemblies such that they revolve and rotate simultaneously. The susceptors are RF-heated and epicyclic motion maintains them at an even temperature.

The Al_2O_3 layers produced by using this technique are reproducible as to physical and electrical characteristics. Figure 11 shows a typical capacitance-voltage (C-V) plot of a 1000 \AA SiO_2 - 500 \AA Al_2O_3 sandwich on 1-ohm-centimeter n-type silicon with aluminum metallization. Test data indicate that the flatband voltages are reproduced within ± 0.2 volt and that shifts in flatband voltage under bias temperature stress nominally are within 0.4 volt, indicating excellent stability.

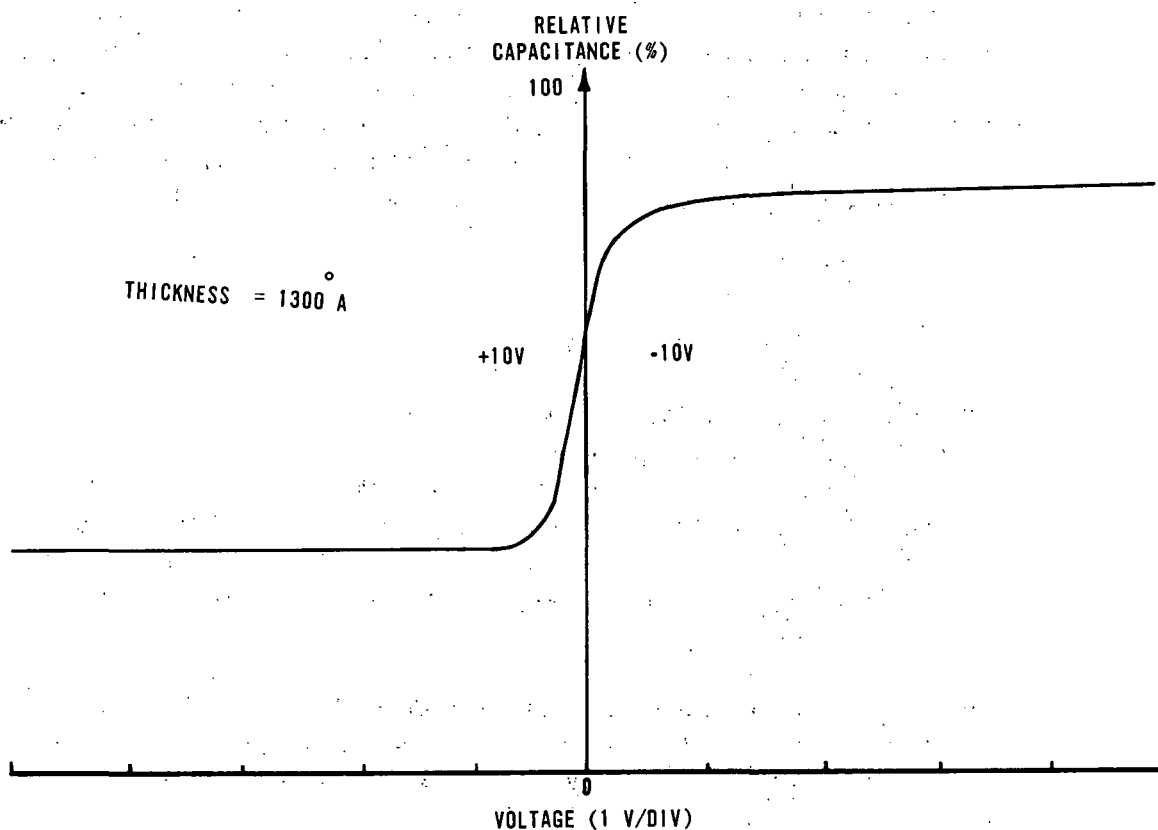


Figure 11. Typical capacitance-voltage (C-V) plot of silicon dioxide and aluminum oxide.

D. Sputtering Dielectric

This method is sometimes called impact evaporation since a surface is bombarded with ionized particles which transmit energy to the atoms or molecules of the surface so that the most energetic ones are emitted. The emitted particles then diffuse to an adjacent surface where they build up a thin-film deposit. Originally sputtering was applied to conductive materials, since dc potential could be established between the target (cathode) and an anode in a gaseous plasma containing positive ions and electrons. The positive ions could then be accelerated toward the target by the potential drop of several kilovolts. Unfortunately, this technique is not generally useful for nonconductive targets, since the accumulated positive charge on the target counteracts the applied dc voltage. This difficulty is circumvented by the application of an RF potential between the electrodes. This method of RF sputtering has recently been developed into a practical deposition process for dielectric films (SiO_2 , Al_2O_3 , Si_3N_4) which have many applications. The alternating potential of the RF input sequentially allows the target surface to be bombarded by positive ions and the positive charge to be neutralized by the highly mobile electrons. This technique is applied to metals and semiconductors.

If the positive ions used in sputtering are not chemically reactive, such as argon⁺ (Ar^+), then little or no change occurs in the composition of the material from target to film. If, however, a reactive gas is present when the plasma is formed, the target surface can form chemical compounds which then become part of the depositing film. This is known as reactive sputtering and is used to produce various films, mainly oxides and nitrides. Likewise, using a gas mixture can result in a film of mixed composition such as silicon oxynitride. Reactive sputtering generally proceeds with a slower rate of deposition than direct sputtering.

One of the most significant recent developments has been the recognition that a considerable amount of resputtering of the deposited film can occur, with important effects on the resulting film properties. Likewise, a quantity of the sputtering gas may be trapped in the film and can cause variations in the physical and chemical properties of the film. Finally, the development of phenomenological models to explain the emission of material as well as the electrical behavior of a sputtering system allows the technique to be generalized to the point where it is probably applicable to a wide variety of materials, rates of growth, and film properties than any other method.

E. Thermally Grown Silicon Dioxide

SiO_2 can be grown using steam in a resistance-heated furnace tube with a Mulite liner. The temperature is usually around 1150°C ; however, it may vary from 900 to 1200°C for MOS devices. For an extremely clean SiO_2 layer, about 0.1 percent HCl is added to the steam. The HCl helps tie up any sodium ions in the tube. Sodium ions are very harmful and may cause the threshold voltage to shift under temperature and bias. After the wafer is thoroughly cleaned, it is oxidized at 1150°C using an oxidant of oxygen (O_2) by itself or with steam. The O_2 combines with the silicon to form a layer of SiO_2 . The growth rate is dependent on the temperature of oxidation and the type of oxidant (dry O_2 or steam).

III. SURFACE PASSIVATION FOR MONOLITHIC CIRCUITS

A. Introduction

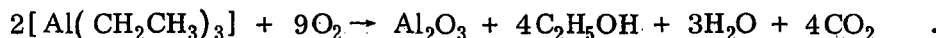
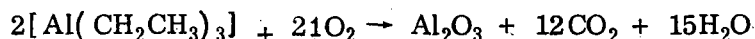
Passivation methods for hermetic sealing of semiconductor devices are generally divided into vapor plating, vacuum, and organic techniques. Vapor plating techniques for depositing various types of glass films for semiconductor passivation applications are the most successful passivation methods related to integrated circuits. Therefore, most of the data presented herein concerns vapor plating techniques. Passivation using electron beam deposited quartz is briefly discussed.

B. Vapor Plating Techniques

Vapor Plating is a process in which a gas compound or gas compound mixtures react at a surface to deposit a low vapor pressure film. Thermal decomposition of single compounds in the vapor state is more commonly referred to as pyrolysis. The basic criteria for vapor plating to occur are (1) the starting reactants must be in the vapor state or easily converted to the vapor state, (2) the primary reaction must take place at a designated surface, (3) the product of the reaction must be stable at the reaction temperature, and (4) any byproducts of the reaction should possess a high vapor pressure to prevent contamination of the low vapor pressure deposit.

Vapor plating, as used for the passivation of semiconductor devices, is illustrated by the mixing of an aluminum alkyl with O_2 or an oxygen-containing

compound to form an amorphous film of Al_2O_3 at a surface held at an elevated temperature. The primary reactions that participate in this vapor plating process are:



From these basic reactions, numerous vapor-plated compounds have been developed and used for the passivation and product improvement of semiconductor devices.

A composition glass is formed by using aluminum alkyl in conjunction with tetraethyl orthosilicate (as a silica source) and/or triisopropyl orthosilicate (as a silica source) and/or triisopropyl borate (as a boron oxide source). The combination of these chemicals has produced the most successful low temperature oxide in use to date. This compound designated as $\text{B}_2\text{O}_3 \cdot \text{Al}_2\text{O}_3 \cdot \text{SiO}_2$ and called boro aluminosilicate, combines many highly desirable dielectric properties into a single glass film which could only be formed from the vapor state. The deposition temperature of 300 to 400° C allows high compatibility with almost all current semiconductor technology.

Vapor plating techniques fall into two broad categories which are based on the source used for silicon.

1. Ethyl Silicate Systems. Ethyl silicate systems use tetraethyl orthosilicate (ethyl silicate) as the silica source. These systems are limited in their applications by the high substrate temperatures required and by slow deposition rates.

In the early process, research and development of vapor plated dielectric films were carried out with various one-component systems; from these one-component glasses, several binary and ternary glasses evolved. The various glasses which have been used for passivating agencies are:

SiO_2	Silica
Al_2O_3	Alumina
$\text{Al}_2\text{O}_3 \cdot \text{SiO}_2$	Aluminosilicate
$\text{B}_2\text{O}_3 \cdot \text{Al}_2\text{O}_3 \cdot \text{SiO}_2$	Boro aluminosilicate
$\text{B}_2\text{O}_3 \cdot \text{SiO}_2$	Borosilicate

A single deposition system is capable of producing any one of these glass films. The major vapor-deposited glass film now used is boro aluminosilicate. This film has been evaluated under numerous types of environmental and long-term reliability tests with different processing variables. It was widely used during its development in all phases of semiconductor technology.

2. Silane Systems. Another vapor-deposited glass film is based on the use of SiH_4 as the source for silicon. The more chemically reactive SiH_4 produces hard and adherent films of high purity SiO_2 at very moderate temperatures. The apparatus for deposition of SiO_2 films from SiH_4 consists of a reaction chamber in which the reactive SiH_4 was synthesized in a controlled manner, a plating head in which the vaporized silicon compound is mixed with oxidizing gases, and a substrate heater which supported the substrate below the plating head and maintained the substrate at a desired deposition temperature. The major advantage of the SiH_4 system depositions is the ability to reach deposition rates in the range of 2000 and 5000 Å per minute, with the possibility of lower substrate temperatures.

C. Borosilicate Silica Glassing

In the manufacture of semiconductor transistors and integrated circuits, it is necessary to provide protection against contaminants that can degrade the electrical characteristics of the devices. Moisture is considered the main agent which must be kept away from the surface. For silicon devices, it is common practice to provide a passivating coating of SiO_2 , usually by thermally oxidizing the surface of the silicon. Thermally grown SiO_2 imparts to the device surface a remarkable degree of passivation but it is not always adequate to preserve initial device characteristics for an indefinite time and under a variety of ambients. Its molecular network structure is relatively open and not impermeable to contaminants. Thick layers of SiO_2 lack mechanical strength because of the thermal expansion mismatch with the substrate. In addition, the layer must be open to permit contact to be made to the device. These open areas are particularly susceptible to contamination from the ambient. Accordingly, oxide-protected devices are sealed in metal cans or in ceramic flat packs. Sometimes, at some risk, they may be embedded in polymeric plastic materials. Both of these encapsulation techniques have disadvantages. Metal can structures and ceramic packages are expensive and occupy such large volumes that much of the potential advantage of small size provided by integrated circuit technology is not realized. Plastic encapsulants, under certain situations, are not impervious to contaminants. Moreover, these materials often act as, or contain, contaminants themselves.

Silicate glasses are recognized as a solution to most of these encapsulation problems. Various methods of applying glass coatings to the surface of semiconductor devices have been proposed but have met with only limited success. For example, fusion techniques have been developed in which the glass is applied to the device surface as a frit that is heated to a temperature above its softening point. The temperatures required for applying the coatings by these methods are often so high that they are restricted to special high temperature metallization systems or to glassing prior to metallization which must then be of limited thickness so that patterns can be etched in these with sufficient precision. Special low temperature glasses have been derived for glassing conventionally metallized silicon devices but they are more or less moisture sensitive. Other known techniques for forming glass layers include reactive sputtering and RF sputtering but these generally must be restricted to simple glass compositions and the deposition rates are low. Furthermore, annealing after deposition is generally required if dense, impermeable films are to be obtained.

Recent efforts in industry have been concentrated on developing a glassing technology free from these various drawbacks. The objective was to devise a batch process, based on chemical vapor deposition at low temperatures, for hermetically glassing semiconductor devices in wafer form. This type of glassing can be considered a key to a simple and much less expensive package because the glass layer serves as the hermetic seal and the costly sealed metal cans and ceramic flat packs are no longer required.

The individual metallized chips can be attached to an inexpensive header in conventional fashion, or they can be mounted face down either on a suitable fanout pattern or directly on a printed circuit board. The completed transistor or integrated circuit package might, for instance, be coated with a plastic polymer for mechanical protection of the package, to shield it from light, and to act as a first barrier against gross contamination.

Inexpensive plastic and ceramic substrate holders with metallization fanouts have been developed on which the glassed chips can be mounted by solder reflow or ultrasonic bonding techniques. Thus, all contacts on a chip can be made simultaneously in one operation, in contrast to the individual wire bonding of each contact now conventionally used.

In addition to the primary purpose of chemically vapor-deposited glass films (i.e., to provide an impermeable insulating and passivating coating), they are useful as an air isolation layer in preparing crossover patterns. As circuit design becomes more sophisticated, these and other applications of

vapor glassing will become essential, especially for computer arrays of higher device speeds in high density with improved reliability and low costs.

D. Glass Deposition

Glass deposition from the vapor phase by chemical reaction has the following distinct advantages over the previously described methods:

1. A relatively low substrate temperature is required for film deposition. The glass compositions are synthesized well below their softening temperature. This low-temperature feature is important because changes in diffusion profiles are prevented or minimized, deleterious effects such as oxidation of the metal leads are avoided, and impurities on the surface are prevented from diffusing into the interior of the device.
2. A wide choice of compositions of high purity can be prepared by controlled variation of the vapor composition. The compositions can be tailor-made to provide desirable properties, such as a matching thermal expansion coefficient. Glass compositions of high purity can readily be made because the reagents used are of high purity, and contamination during deposition and subsequent handling can be made negligible.
3. Integral films with gradually or abruptly changing compositions can be prepared in one deposition operation simply by changing the reactant vapors introduced into the reaction chamber.
4. The film thickness can be readily controlled. For example, on silicon substrates, glass thicknesses ranging from 500 to 250 000 Å have been reproducibly deposited.
5. The film thickness is highly uniform over the exposed surface of a device, regardless of its shape. Furthermore, film deposits are virtually free of pinholes and cracks. The films can also be deposited in selected areas of a wafer through appropriate masks.
6. The processes for depositing the films are economical and practical because fairly high film growth rates can be achieved. The deposition equipment is relatively simple and can be scaled up for large scale batch production.

7. The dielectric and chemical properties of the glass films and their hermeticity can be additionally improved by a brief heat treatment at a temperature above the deposition temperature. The delineation of patterns by photomasking and etching methods may be carried out on undensified layers which exhibit greater solubility than densified films.

8. The adherence of vapor-deposited glass films to metallic surfaces, such as tungsten metallization on devices, is much better than for glass films deposited by fusion techniques. The quality of the glass-to-metal seal should, therefore, be superior.

The principal disadvantage of the chemical vapor glassing process is the care required to control the proper reagent flow rates. If they vary, improper composition of the film results. A second disadvantage is that the reactants are toxic and flammable.

Two main types of chemical vapor glassing have been developed and are distinguished as follows:

1. High temperature (700 to 800° C) reactions with organo-metallic reagents employing an open furnace.
2. Low temperature reactions (275 to 475° C) with inorganic reagents in a rotary (hot plate) reactor.

The high temperature processes are based on organo silicon compounds, such as tetra ethoxy silane, as sources for the silicon component in the glasses, whereas the low temperature processes use SiH_4 to provide the silicon.

The SiH_4 -based, low temperature systems have considerable advantages over the older type systems and have, therefore, been developed to a much greater degree of refinement.

The most satisfactory compositions developed for silicon device glassing are:

1. The borosilicate compositions synthesized from SiH_4 , diborane (B_2H_6), and O_2 which are readily prepared and are satisfactory for most purposes of device glassing.
2. The alumino borosilicates from SiH_4 , B_2H_6 , trimethyl aluminum, and O_2 which are more difficult to prepare but offer improved chemical stability.

3. Laminates consisting of combinations of borosilicates or aluminoborosilicates and SiO_2 , with or without base layers of Si_3N_4 .

Various processes of glass deposition from the vapor state are discussed. Included are SiO_2 , borosilicates, aluminosilicates, phosphosilicates, and laminates.

1. Silicon Dioxide. SiO_2 is the most commonly used single component glass. It can be deposited by the thermal decomposition of SiH_4 with O_2 at a preferred temperature in the range of 450 to 475° C. Lower temperatures (down to 250° C) can be used but deposition rate and film quality decrease. Although SiO_2 gives a remarkable degree of passivation, its relatively open molecular structure is not sufficiently closed to contaminants. For this reason, SiO_2 passivated devices must be sealed in either metal or ceramic packages. Thick layers have little mechanical strength due to the thermal mismatch between SiO_2 and the substrate. The reaction for thermally deposited SiO_2 from SiH_4 and O_2 is



2. Borosilicates. Borosilicates (binary component glasses) are deposited from the reaction of SiH_4 , B_2H_6 , and O_2 at a temperature of 450° C. Compositions with different thermal expansion coefficients, softening points, etch rates, etc., are possible. For example, compositions obtained from 20 to 25 volumes of pure B_2H_6 and 75 to 80 volumes of pure SiH_4 are most suitable for silicon device passivation. Compositions obtained from 25 to 30 volumes of B_2H_6 and 70 to 75 volumes of SiH_4 give the best thermal expansion match for silicon. These films are similar to the commercial Pyrex type borosilicate glasses but they contain no alkalis and are of higher purity. Films up to 25 μm thick have been deposited without defect formation. Deposition rates up to 2400 Å per minute have been reached, although the rate of 5 to 6 μm per hour is preferred.

3. Aluminosilicates. The aluminosilicates (ternary component glasses) are deposited from the reaction of SiH_4 , B_2H_6 , trimethyl aluminum, and O_2 . They have excellent chemical and physical properties. The Al_2O_3 gives the glass a greater stability and inertness than the borosilicates. This glass is not as clean as the borosilicates but etches at similar rates and has excellent dielectric and hermetic properties.

4. Phosphosilicates. Phosphosilicates [prepared from phosphine (PH_3) SiH_4 , and O_2] are hygroscopic and do not densify with heat treatment. They do have some use in laminates.

5. Laminates. The most commonly used laminate is a layer of SiO_2 over a thick layer of either borosilicate, aluminoborosilicate, or phosphosilicate glass. The most useful is SiO_2 over a borosilicate.

E. Thermal Densification of Glass Films

The glass films deposited at the usual low temperatures have remarkably good properties and are satisfactory for certain applications, but a distinct enhancement of the film properties can be achieved by a brief heating at an elevated temperature to form dense, stable, and more chemically resistant glasses. This effect appears to be based primarily on a change in the bonding between the silicon-oxygen linkages, resulting in a consolidation of the molecular structure. The effects of these changes can be observed in the infrared spectra, chemical stability, dielectric breakdown strength, density, and especially the dissolution rate which decreases sharply. Most glass films deposited by chemical vapor reactions and RF sputtering techniques, including the SiO_2 and Al_2O_3 films, have been found to undergo densification except the films deposited from mixtures of SiH_4 and PH_3 . The effects of densification on SiO_2 films have recently been measured in some detail by several investigators.

The degree of densification of most deposited glass films is a function of temperature, time, and ambience. O_2 exerts an accelerating effect. Temperatures below the softening point of the glass should be chosen to retain the integrity of the film structure. At a given temperature, densification is rapid initially and then tapers off until changes become negligibly slow.

F. Substrate Materials for Glassing

The glass synthesis processes that have been described are applicable for coating of a wide range of substrate materials. The properties of the glasses are readily adjustable by changing the vapor composition, making it possible to tailor make coatings with thermal expansion properties that closely match those of the substrates. The thicker the coating that is required, the better the thermal expansion match must be. Films up to a few thousand angstroms thick need not match closely, especially if the expansion coefficient of the film is lower than that of a much thicker substrate, i. e., the film is under compression. SiO_2 films on silicon are a good example.

Another requirement for successfully glass coating a given substrate material is that it must be thermally and chemically stable under the glassing

conditions. Aluminum reacts slightly with borosilicates and strongly with phosphosilicates during glassing reactions that employ the hydrides necessitating the deposition of a thin protective layer of SiO_2 preliminary to the binary glass deposition to prevent the formation of difficult soluble interfaces that may interfere in metallurgical bonding.

The following materials have been successfully glassed using the standard rotary reactor glassing techniques: silicon ceramic compositions, fused quartz plates, silicate glass plates, silicon nitride, ferrites, alumina, tungsten, molybdenum, Kovar, nickel, copper, silver, chromium, steel, aluminum, platinum, and gold.

G. Passivation Using Electron Beam Evaporated Quartz

Quartz (SiO_2) glassing, evaporated using an electron beam, provides a protective overcoat that prevents shorts from loose metal particles in the package. The quartz is deposited approximately 10 000 Å thick. The deposition is made by continually feeding a quartz rod into an electron beam gun. Quartz glassing can be applied to the metals, oxides, and nitrides on the chip. Areas that must remain clear (bonding pads, beam leads, etc.) can be coated with photoresist before glassing. Firing in a furnace explodes the photoresist away from the metal, disintegrating the glass layer over the photoresist. This clears the area for bonding and improves the thermal and electronic contact between the bonding head and chip metal. SiH_4 deposited SiO_2 on silicon monoxide (SiO) can be used instead of quartz glass for the protective layer. Vacuum deposited glass systems are considered to be electrically sound but are expensive.

H. Passivation Using Sputtering

Reactive sputtering of metals to deposit metal oxide insulating films can be accomplished with glow discharge powers up to 3000 watts. A water-cooled substrate holder is needed in order to prevent excessive substrate heating in preparation for the glassing of active devices. A cathode suppressor electrode is used to eliminate arcing and provide higher current densities. Flowmeters are used to allow controlled metering of gases admitted to the sputtering chamber. The sputtering chamber is evacuated and silicon can be reactively sputtered in a 50-percent Ar, 50-percent O_2 atmosphere to produce deposited films of vitreous SiO_2 . Figure 12 is a schematic representative of the apparatus.

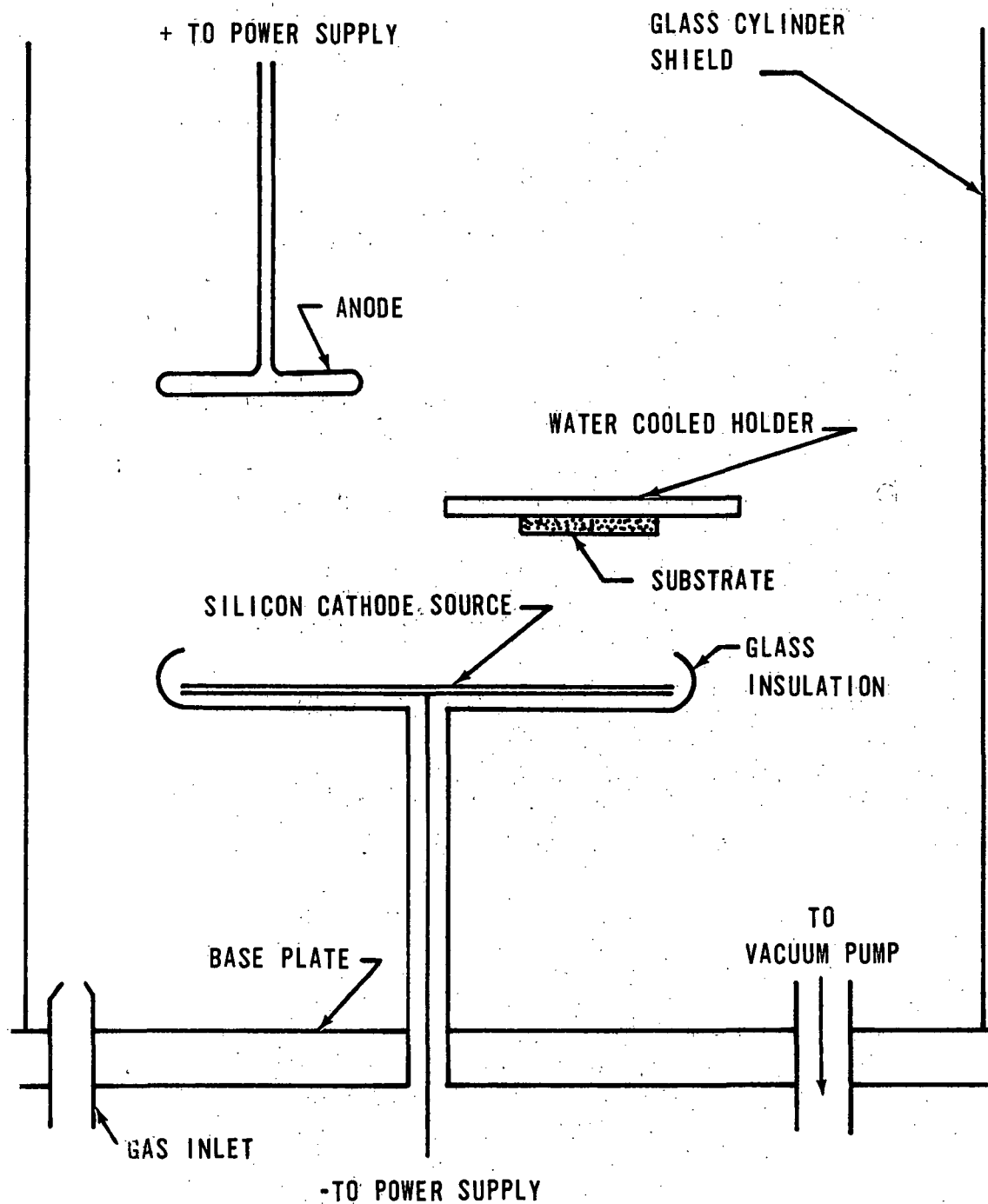


Figure 12. Sputtering system.

With pressure maintained at 10 and 20 μm and a discharge power of 500 watts (2000 volts, 250 mA) a film of approximately 1000 Å thickness was

produced in a 4-hour period. The film of SiO_2 when evaluated as a capacitor dielectric on two ceramic substrates with evaporated aluminum electrodes, exhibited dc leakages on the order of 10^{-9} A/cm^2 at 25 Vdc.

Oxide-mask diffused transistors with a coating of SiO_2 have been step-stress aged. Test data from this evaluation indicate that the sputtering technique is not the most satisfactory method for integrated circuit and transistor device passivation.

In general, vacuum techniques, including sputtering, do not offer a suitable method for large area passivation of transistors. Sputtering systems generally give electrically poor results with degradation of transistor properties. However, in recent months it has been reported that little change in threshold voltage has occurred in low energy sputtering on MOS devices passivated with Si_3H_4 and having silicon gates.

IV. METALLIZATION FOR MONOLITHIC CIRCUITS

A. Introduction

Recent advances in the manufacture of complex integrated circuits have led to a variety of techniques for metal interconnection on the chip. As the need for more and more devices has increased chip size, the problem of random defects has become catastrophic. Functional yields are often seen to drastically decrease or even vanish with attempts to fabricate very large integrated circuits.

Since the major factor determining die size is the metal interconnect size and spacing, one way to conserve space while achieving highly complex circuits is to employ more than a single layer of interconnection metal. At present both double- and triple-layer schemes are being used. These multilayer metallizations, while solving the problem of chip defects, have serious drawbacks which are discussed herein. The multilayer systems considered are all aluminum based, i. e., pure aluminum or lightly doped aluminum. Although other metals are being experimented with, aluminum systems make up almost all of the commercially available integrated circuits at this time. In general, these metal layers are insulated from one another by a deposited dielectric, usually SiO_2 .

The most prominent yield limiting problems are discussed. These include coverage of both metal edges and oxide steps with additional metal and/or another layer of oxide. Processing parameters such as profiles, thickness, temperature, composition, etc., that influence coverage are discussed as well as innovations for improving less-than-desirable results.

A class of problems related to the presence of via holes or oxide windows for interlayer continuity is presented. In addition, the problem of random defects such as pinholes and inclusions in the oxide insulation layers is mentioned. Finally, these data are related to the tradeoffs that occur in building up additional layers or increasing die size.

The demands of highly sophisticated electronic systems have pressured the semiconductor industry into placing more and more devices on a single chip. This has resulted in a large scale integration (LSI) of previously hybrid designs and led to the emergence of enormous die sizes. The process engineer has seen this new complexity result in drastically reduced circuit probe yields at a time when less circuits per wafer are available.

If increased complexity is demanded and defect levels are fixed, attempts must be made to maintain as small a chip size as possible. Since device sizes are determined by certain performance requirements, the conservation of die area must be achieved by modifications to the interconnection scheme. Current density considerations and photolithographic processing fix the stripe cross section, width, and spacings. Therefore, to further conserve chip space, one or more additional layers of metallization may be necessary.

B. Multilayer Metal Process

A multilayer metal system consists of three metal and three insulation layers. The metal is aluminum based, evaporated at a pressure of less than 10^{-6} torr, with substrate temperatures in excess of 250°C and rates greater than 100 \AA/s . These parameters are determined by the specific deposition system used and are established so as to yield a large-grained ($>4\text{ }\mu\text{m}$) and uniform film, particularly at steps in the underlying oxide. The layers are successively thicker, and the deposition conditions are changed to achieve consistent film parameters from one layer to the next.

The insulation is a phosphorosilicate glass deposited by standard CVD techniques. The phosphorous content is about 1 percent by weight. Deposition is accomplished at temperatures in excess of 425°C , at rates of approximately

1000 Å/min. Glass thicknesses and composition have been determined by profile studies to yield oxide steps readily covered by subsequent metal.

The interlayer vias are patterned by standard photoengraving techniques and etched with any of a variety of fluoride-based etches designed for accurate pattern reproduction with limited attack on the metal.

The circuits involved are sample probed after the patterning of each metal layer to ensure integrity to that point. Process control patterns are included on each wafer and are designed to yield detailed information about each metal layer. Interlayer contacts are also probed during processing as a monitor on circuit quality.

C. Metal Coverage

The continuity of metal interconnections has been one of the most formidable problems encountered in the manufacture of semiconductor circuits. The cause of the problem is the lack of planarity of the circuit's surface. Steps in the insulating oxide at metal edges and oxide windows present a variety of surface contours which range from beveled to very sharp and can be difficult to cover uniformly with metallization.

Three types of edge contours are found when standard metal processing is employed and no special processes for edge beveling are used. These are: (1) the via edge; (2) the metal crossover; and (3) aligned first and second metal edges. The steps into the windows are very similar to the ohmic contact regions found in single-layer circuits. No special processing tricks are necessary to achieve the uniform bevel of the oxide. The degree of the bevel, however, appears to be dependent upon the dopant level in the glass, increasing as the dopant concentration goes up.

The step created by the edge of a passivated metal stripe is dependent upon both the metal edge profile and the deposited oxide's replication of that profile. However, these steps tend to be vertical, as discussed in the following section, and quite difficult to cover with subsequent metallization. The distinction between the open and the well-covered edge is quite clear. To achieve the coverage it is necessary to use the deposition parameters previously described: rates in excess of 100 Å/s and substrate temperatures greater than 250° C. Both slow rates and low temperatures reduce the surface mobility of the freshly deposited aluminum and tend to yield poor coverage in varying degrees.

A formidable situation arises in the manufacture of three-layer parts when the edges of a first- and second-layer metal stripe coincide, either by design or error. This results in an exceptionally large and steep step over which it is very difficult to deposit a continuous metal layer. Metal step coverage problems and cracking are shown in Figure 13. In fact, the step has resulted in a completely open stripe. When the deposition temperature is increased, the coverage is improved.

In addition to the use of high temperatures and fast deposition rates, processes can be designed which shape both metal and oxide edges. When shaping oxide edges in multilayer technology, the risk of introducing a multitude of pinholes exists. These pinholes result in interlayer shorts. Processes that chemically bevel insulating oxide edges over metal steps are, therefore, not recommended. It is possible, however, to produce smooth oxide profiles by shaping metal edges beneath them. Beveling processes can be performed on first-layer metal which result in ideal metal coverage at the second layer. Furthermore, the beveling of first-layer metallization places less stringent requirements on the deposition parameters for the subsequent metallization. This results in less need for sophisticated vacuum coaters for the second and third metallizations.

In recent months much attention has been devoted to the application of anodization techniques to multilayer systems. A so-called no step two-layer metallization appears to be possible. Indeed, the use of anodic films for complex structures will most likely be widespread within the next year. Since multilayer data are sure to appear and be of great interest to those who have worked to achieve improvements in circuit metallization.

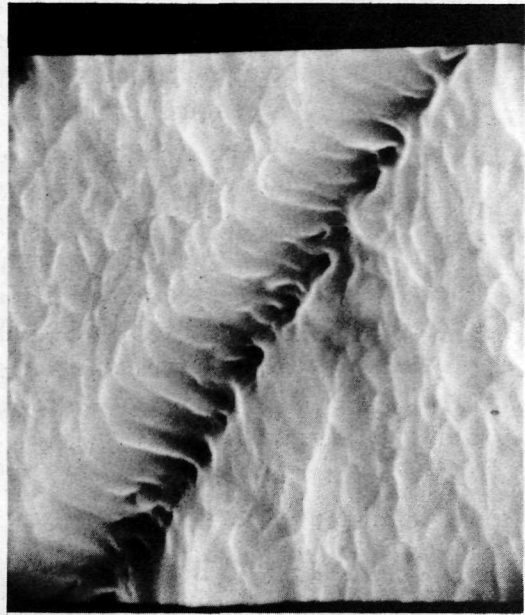
Finally, the role of surface cleanliness for improvement in metal coverage cannot be over emphasized. In addition to the use of heat and fast rates to increase metal mobility, clean surfaces prior to deposition are a necessity. Although several wet chemical means exist for achieving clean surfaces, the use of plasma cleaning or sputter etching appears to be finding widespread application today. Any method that promotes good adhesion, high mobility, and, hence, a good coverage is acceptable.

D. Effect of Substrate Temperature on Film Deposition

It has been found that the temperature of the substrate during vacuum deposition plays a significant role in determining the final characteristics



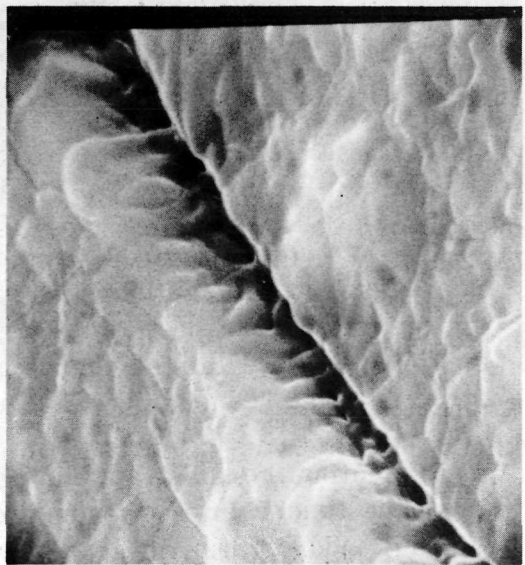
a. Device S/N 00110,
tilt 60 deg, 5000 X.



b. Device S/N 00110,
tilt 60 deg, 20 000 X.



c. Device S/N 00111,
tilt 60 deg, 2000 X.



d. Device S/N 00111.

Figure 13. Metal step coverage and cracking (SEM photographs of Raytheon 709 type devices, submitted by General Dynamics/Convair, device lot 7111).

of the deposited film. Shown in Figure 14 are three photomicrographs of deposited aluminum on a SiO_2 wafer. Aluminum was deposited to a thickness of 12 000 Å at room temperature, 175° C, respectively, and all photographs are at 10 000X magnification.

At the boundary layer between the deposited aluminum and the silicon dioxide substrate, a stress exists which has a tendency for forming dislocations. Hillocks, or small irregularities in the normal surface contour, are the results of the stress condition. In addition, since the thermal coefficient of expansion of aluminum is much greater than that of SiO_2 , considerable stress is created during subsequent temperature cycling such as occurs during annealing. These stresses may then create discontinuities and cracks in the surface film.

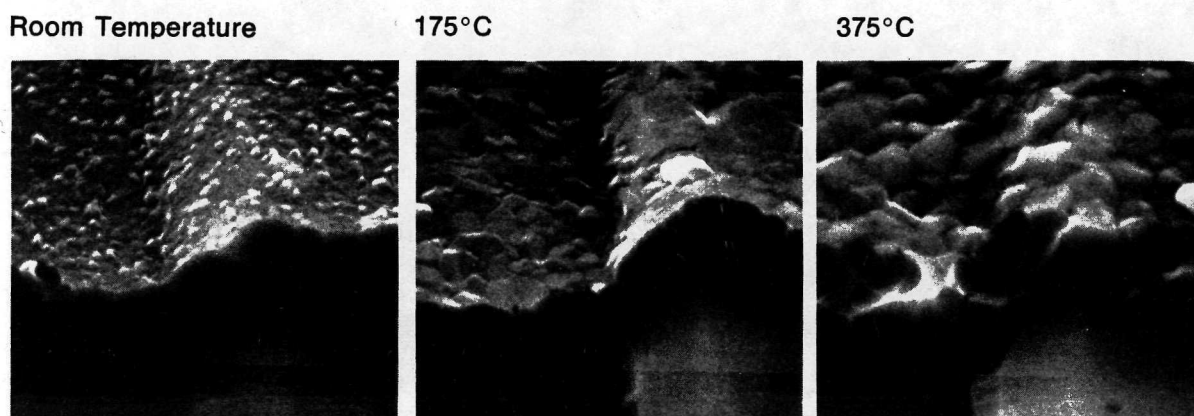


Figure 14. Photomicrographs of deposited aluminum on a SiO_2 wafer.

As the temperature at which the deposition is performed is increased, the average grain size increases and the number of hillocks per unit area significantly decreases. The larger grain structure provides for a more continuous film with less chance of cracking and dislocation. A larger grain structure also reduces overall boundary stress.

Heating the substrate during the deposition process increases the mobility of the condensing aluminum atoms and allows the cracks to heal. This will not occur by heating after the deposition is made because of the oxide which develops on the aluminum surface after exposure to air. Adhesion of surface to surface is also superior at elevated temperature above 150° C.

E. Oxide Coverage

In general, the metal coverage problem was so dominant that oxide coverage was not deemed a problem in the earlier stages of multilayer processing. Since the vapor depositions were at atmospheric pressure where the mean-free path of the reactant species is much less than the step heights over which the oxide must cover and, since the temperature variation from metal to oxide is minimized by conduction and radiation through the thin films, there is no chemical reason why oxide deposition should not occur on the vertical edges of the steps. Recent data indicate that uniform oxide coverage is generally not the case and that underlying surface material, geometries, and thicknesses can have effects on oxide profiles.

For nonbeveled metal strips, oxide profiles are affected primarily by the ratio of oxide-to-metal thickness for a given deposition rate. Although thin oxides generally covered the metal step adequately, they are prone to excess pinholes and are not discussed.

A threefold solution to the problem exists. First, the ratio of oxide-to-metal thickness can be increased. Here the thickness ratio is about 1.3, and the cusped step has been eliminated. Second, the deposition rate can be decreased. For rates on the order of 200 to 300 Å/min some improvement is made in the oxide profile. However, the increase in run time to achieve comparable oxide thicknesses makes this approach less desirable. The oxide profiles can be significantly altered by tailoring the underlying metal edge. This perhaps produces the most dramatic effect of varying degrees of metal edge bevel on oxide coverage. The completely beveled metal edge produces a very uniform oxide coverage.

The effect of glass composition on oxide coverage was shown to be small. Glasses containing amounts of phosphorus from 0 to 10^{21} atoms/cm³ produced essentially the same deposition characteristics on the profile. As one would expect, however, the etch characteristics varied widely, and so any profiling by etching is controlled by the oxide composition.

F. Vias

A unique problem encountered in the manufacture of multilayer circuits is the reliable etching of many small interlayer vias. For the contacts to function properly they must maintain the low resistance of the individual metal

layers. It is important to have a highly reliable via etch process since the malfunction of a single via results in the loss of the circuit. In relatively simple three-layer parts (100 vias/layer) it is apparent that exceptional via yields are necessary (99.2 percent). Furthermore, in complex circuits (more than 500 vias/layer) very low yields will result unless the via process is of exceptional quality (99.8 percent yield).

Assuming photomasks of acceptably high quality are obtainable, the basic problem encountered in the via process is in the oxide etch which cuts open the via holes. Since both underetching and overetching are disastrous, the process must be exceptionally well controlled.

Because of the reactivity of aluminum with a wide range of the fluoride-based etches used today and the lack of absolute oxide uniformity, control over etching the via holes and removing the underlying metal is a common problem. In addition, certain circuit contacts appear to accelerate the corrosion of the metal. While one area appears unattacked, others may be seriously corroded. The first-layer metallization was completely removed during the via etch process or in the preparation for second metal deposition. Upon deposition of the second-layer metal, two voids were created under the lip of the via edge where the first-layer metal was removed. This results in an open-circuit when the first metal to second metal contact is probed. In most cases complete removal of the metal does not occur. The metal is thinned, producing a high-resistance contact. The thinning is not detectable by optical means, making the problem difficult to observe.

In attempting to correct or compensate for this problem, the reverse effect is sometimes seen; the deposited oxide is not completely removed from the via window. The detection of this problem is difficult by optical means since the oxide layer is often less than 250 Å thick.

G. Other Defects

In addition to the coverage and via problems, other random defects are extremely troublesome in multilayer processing. Many processing defects can be directly connected to the presence of defective patterns on masks. Some percentage of the defects used estimating yield losses could be eliminated by improvement in mask quality rather than process innovation.

In single-layer processing, where the passivating dielectric is used primarily as a scratch protection layer, the occurrence of pinholes — whether

through faulty masks or processing — is not really a problem. However, in multilayer processing each pinhole represents a potential interlayer short and, hence, a defective circuit. Process control is a necessity to keep the pinhole density as low as possible. One control on the pinhole count is to insure that certain oxide thickness criteria are met. Catastrophic pinhole counts (greater than $4/\text{cm}^2$) almost always occur when surfaces are improperly prepared or the oxide thickness is less than 2000 \AA . The use of proper cleaning prior to glass deposition is essential for keeping interlayer shorts due to pinholes down to a minimum.

Another cause of interlayer shorts is the growth of hillocks (bumps in the metal) after the deposited metal is thermally cycled. It is not unusual for these hillocks to occur in densities on the order of $10^6/\text{cm}^2$ and to grow to heights of 7 to $10 \mu\text{m}$. Failure of the passivation or photoresist to cover these hillocks can result in etched holes in both the metal or the oxide. Since the glass covering the hillocks is often cracked during the via exposure sequence, the etch process produces serious oxide flaws which result in catastrophic interlayer shorts when subsequent metallization is performed. Hillocks are believed to be a manifestation of creep in the aluminum film caused when the film is heated on a substrate. This places the film under compressional stress. The density and size of hillocks have been related to the grain structure of the film, its composition, and the time and number of thermal cycles which the film has undergone. In general, it has been shown that hillock density and size decreased when increased grain size and increased doping aluminum. A reduction in the temperature which the evaporated film sees in subsequent processing will also prevent hillock growth. It is interesting to note that the use of a low-temperature passivating coating ($<400^\circ \text{C}$) is very effective in preventing hillock formation. Layers as thin as 1000 \AA of SiO_2 will eliminate the problem regardless of the subsequent processing which the film receives.

Since the density of hillocks formed is so great and since a single hillock can result in catastrophic shorts, this problem must be eliminated before reasonable circuit yields can be expected.

In addition to hillocks and pinholes a certain random defect level will be generated by normal processing and handling operations. It is difficult to number them since they vary widely depending upon the system employed. It is sufficient to say that the effects of handling can be minimized if handling itself is kept to a minimum. Mechanization and automation of many of the hand operations will result in a decrease of this type of defect.

H. Process Control

The present degree of circuit complexity often makes it impossible to relate circuit failures to process problems either by directly probing the circuit or by visual observation. The defect site simply cannot be detected by observing the circuit failure mode. Probing within the circuit itself is almost impossible when three densely packaged metal layers are used. A practical solution of the problem of relating the failure to its defective process lies in the use of patterns that simulate circuit geometries, but which contain tests subject to a single failure mode. For example, if one observes a circuit failure due to an interlayer open, it is difficult to decide from the device itself whether the failure has been caused by metal coverage problems or by via resistance. It is relatively easy, however, to design a test pattern which treats the two problems independently and, hence, allows corrective information to be fed back into the wafer process area. The design of the test pattern must correspond to the complexity of the circuit if these patterns are to be useful. If one has a circuit containing 1000 via holes between first- and second-layer metal, it is senseless to use a via test pattern that tests 100 vias. A process failure rate of 0.1 percent will cause nearly every circuit to be rejected while all via test patterns will probably appear good.

Test patterns should be employed on all circuit wafers. The number and complexity of these is determined by the circuit complexity and the specific process sequence employed. The process control pattern serves a threefold purpose. First, it aids the failure analysis of very complex circuits. Second, it allows the process engineer to constantly monitor the process parameters that must be kept uniform over long periods of time. Finally, it allows in-process judgements to be made on the quality of material in process and permits rejection of bad material to occur as early as possible in the process, saving additional costly processing steps.

The problem of hillocks, which can be ignored for single-layer circuits, becomes great when multilayer metallization is employed. Interlayer shorts causing essentially zero-circuit probe yields are often the result of poor control of hillock growth. Using large-grained aluminum films for all metal layers, and restricting thermal cycling of the metal in an unpassivated state can keep the problem minimal and reduce interlayer shorts.

Process control patterns are essential to monitor circuit quality, to perform failure analysis, and to assist in process development. These

patterns must correspond to the individual circuit's complexity and must test each process failure mode.

I. Metal Sputtering on MOS Devices

It has been reported that low voltage metal sputtering can be performed without detrimental effects on silicon gate MOS devices if they have been coated with Si_3N_4 previously. Without silicon gates and Si_3N_4 , sputtering can be accomplished; however, the devices must be annealed afterward. The amount of annealing usually required for device sputtering depends on the voltage level at which the sputtering occurred. For low voltage sputtering on MOS devices annealing of 1 hour at 400°C is usually required. For high voltage sputtering a longer period is required, usually 2 to 3 hours at 400°C . This type of annealing will most often result in lowering the threshold voltages to the original values or to slightly increased values. Sputtering of thin films of platinum, molybdenum, titanium, tungsten, and tungsten-titanium alloy for beam lead MOS and bipolar integrated circuits is presently being done by several large semiconductor companies.

J. Characterization of Thin Films

The control of thin-film properties requires a number of methods of measuring the properties of the film. In some cases, this may be done even during deposition but most evaluation is performed afterward. The refinement of measurement methods has been responsible for much of the recent technological advancement in the use of thin films. The rest of the discussion will deal with measurements directly involving the films themselves.

1. Thickness. A very basic parameter is the thickness of the film. Its value is predetermined by a knowledge of the deposition or growth rate as a function of the parameters of the deposition system (power, temperature, pressure, etc.). In some cases, the actual thickness can be measured in situ during deposition. The optical absorption of a transparent film can be monitored during evaporation or sputtering. For other films, indirect rate monitoring methods employing a previously calibrated system are used. However, when the deposition is complete, it is desirable to be able to measure the actual film thickness. This is normally done by physical or optical methods. The simplest physical method employs a sensitive stylus which is allowed to glide over the surface until the edge of the deposited film is encountered. The step height thus directly measured is the film thickness.

Of course, only the thickness at the edge can be measured. Other more complex methods have been developed such as the absorption of beta-particles of known energy. Finally, if the relative dielectric constant of an insulating film is known, an estimate of thickness can be made from the measured capacitance of the film between two suitable electrodes of known area. The latter method, though cumbersome, is often useful in cross-calibrating other methods.

Most of the methods for transparent or translucent films are optical techniques which utilize either absorption or interference of light to make the measurement. A simple rapid method for measuring the thicknesses of nonabsorbing films is by variable amplitude, multiple fringe observation (VAMPU) which is suitable for films from several hundred to several thousand angstroms but requires a relatively large area. An even simpler method is color comparison of the film to a calibrated sample with various thicknesses, called a step gauge. For accuracy, a calibrated sample is required for each material, since the color change is due to interference which is a function of the refractive index of the material. For thicker films, opaque films, etc., thickness measurements can be made by multiple-beam interferometry. Unfortunately, the requirement of a highly reflecting surface and the need for precision optical equipment make this method more cumbersome.

Very thin films of transparent material may be measured by polarization spectrometry or ellipsometry, in which the phase angle shift of elliptically polarized light being reflected back from the interface of the film and substrate is a function of film thickness and refractive index. This method is most useful for extremely thin films from a monolayer up to several hundred angstroms. Another measurement suitable for very thin films is the Brewster-Angel technique for accurate measurement of refractive index.

2. Structural Properties. The structural details of thin films are of importance in governing such behavior as resistivity, stress, chemical stability, and other more subtle properties which will be discussed in more detail along with reliability. Structural investigations can be simply microscopic observations of grain size, texture, metallographic structure, staining, etc. However, a large number of thin films are devoid of any visible structure and more refined investigatory tools are employed. These include: X-ray and electron diffraction to determine the extent of crystalline structure in the film, scanning electron microscopy (SEM) to determine high resolution surface features, transmission electron microscopy (TEM) to detect internal fine structure, preferential chemical etching, and polarized light for internal stress analysis. If the substrate is transparent to infrared or visible radiation, internal reflection spectroscopy can be used to study the absorption properties of surface films.

3. Mechanical Properties. Actually the so-called mechanical properties are really manifestations of the interaction of physical and structural factors. However, they are conveniently discussed as such, and the most significant are probably stress, hardness, and the coefficient of thermal expansion. Stress is particularly important, since the combination of residual intrinsic stress and that due to expansion mismatch can easily exceed the yield strength of the film and/or adhesive forces, resulting in separation or fracture. Both compressive and tensile stress are common. It is generally preferable to have compressive stress to prevent propagating cracks. Hardness is a measure of the resistance of the material to abrasion and scratching. One of the hardest known thin films is Si_3N_4 . The coefficient of thermal expansion is important because of possibly disruptive forces arising from a gross mismatch between films or between films and substrate.

4. Electrical Properties. For microelectronics, the electrical properties of thin films are of prime importance. No other single characteristic spans as wide a range as electrical resistivity, ranging from $10^{-6} \Omega/\text{cm}$ for the most conductive film to $10^{18} \Omega/\text{cm}$ for the least (SiO_2). In fact, every type of thin film can be characterized by its resistance and one or more electrical properties as shown in Table 2. Recently, considerable attention has been paid to the conduction mechanisms by which thin films of dielectric materials exhibit measurable electrical currents. These currents are nonohmic, and the more important processes are tunneling, field emission, space-charge-limited current flow, and internal field emission. These are shown in Table 3 along with some typical materials.

A model for a metal-semiconductor contact, whether ohmic or not, is a Schottky barrier in series with the spreading resistance of the bulk semiconductor. The metal-semiconductor contact always has an associated space-charge layer whose behavior is nonlinear, but the contact is still ohmic if the space-charge layer impedance is negligible in comparison with the bulk semiconductor resistance. It is assumed that minority carrier injection is either absent or negligible and that trap-charging effects are small. The fabrication of an ohmic contact thus requires a low impedance of the Schottky barrier. There are two current transport mechanisms in Schottky barriers: thermionic emission, and tunneling. These correspond, respectively, to the two main empirical ways of making contacts: choosing a metal which makes a low Schottky barrier with the semiconductor, or doping the semiconductor heavily near the contact so that the barrier will be thin enough to be penetrated easily by tunneling.

TABLE 2. CLASSIFICATION OF TYPICAL MICROELECTRONIC THIN-FILM MATERIAL BY RESISTIVITY AND OTHER ELECTRICAL PROPERTIES

Type	Example	Resistivity (Ω /cm)	Other Parameter
Dielectric	SiO ₂ SrTiO ₃	10 ¹⁸ 10 ¹⁴	tan δ ϵ
Resistor	NiCr CrSiO ₂	10	TCR
Semiconductor	CdS PbTe	10 ⁻³	μ_e
Conductor	Al Mo Pt	10 ⁻⁶	Al-Si J _p Pt-Si barrier height

TABLE 3. MECHANISMS OF ELECTRICAL CONDUCTION IN DIELECTRIC FILMS

Mechanism	Thickness Range, μ	Current Dependence	Example
Tunneling	<0.01	$1 \sim V^2 \exp(-k/V)$	GaSe
Emission, Schottky	0.01-0.5	$1 \sim T^2 \exp(a\sqrt{E}/T)$	Ta ₂ O ₅
Emission, Frenkel-Poole	0.01-0.5	$1 \sim T^2 \exp(2a\sqrt{E}/T)$	Si ₃ N ₄
Space Charge Limited	~ 1.0	$1 \sim V^2/x^3$	
Ohmic		$1 \sim V \exp(-b/T)$	SiO

5. Chemical Properties. The most important property of thin films is their behavior toward specific etchants. This determines the usefulness of the film for, if high-resolution patterns cannot be generated by chemical means, the film is of limited use. The etch rate and the edge resolution attainable with a particular etching process is of great concern. The appropriate etching solutions and procedures for some common thin films are given in Table 4. The etch rate is determined by the film structure, density, impurity concentration, strain, and other factors. A correlation exists between such properties as etch rate and corrosion resistance and observable quantities such as the visible and infrared absorption spectra.

Recently, significant advances in instrumental techniques have been made which allow much finer structural detail to be disclosed. The important new techniques of X-ray fluorescence, electron scanning chemical analysis (ESCA), and ion source spectrometry (ISS) allow, in effect, a quantitative analysis to be performed on the thin film. By using X rays, extreme sensitivity may be achieved in detecting trace impurities. ESCA allows local analysis of a small area, while ISS allows a mass-spectrometric chemical analysis of a monolayer of the film. Somewhat older but still useful methods employ radioisotopes to study film behavior. These can be introduced externally, or generated in the film by neutron activation of natural isotopes occurring in the film. Selective etching and counting of film allows a profile to be constructed of the radioactive substance. These methods have been useful in the study of the distribution of alkali ions and hydrogen in SiO_2 .

An important chemical property of glass films is the ability to resist diffusion of corrosive substances which can attack interconnections, the semiconductor surface, or underlying oxide surfaces. The ability to protect the edges of metallic films is called edge coverage and is critically important in production of multi-interconnection level integrated circuits. Recently it has been shown that there are inherent reasons for the difficulty encountered in edge coverage by evaporated films. Metallic films for use in microelectronics are often judged by such chemical criteria as the thermodynamic stability of their oxides (since this is related to adhesion of the metal to underlying SiO_2) or the physical coherence of their oxides. Coherent Al_2O_3 acts to passivate aluminum films from further oxidation. Copper films, on the other hand, must be protected from formation of copper oxide (Cu_2O), and molybdenum films have as their most undesirable feature that of susceptibility of oxidation corrosion. A summary of some of the more common metals used as thin films is given in Table 5.

TABLE 4. ETCHANT SOLUTIONS FOR COMMON FILMS

Film	Mask	Etch
SiO ₂	KTFR	Buffered HF
Si ₃ N ₄	SiO ₂	H ₃ PO ₄
SiO	KPR	NH ₄ -NH ₄ OH
Si	KPR	HNO ₃ -HF
Al	AZ-1350	H ₃ PO ₄ -HNO ₃
Au	AZ-1350	KCN-H ₂ O ₃
Mo	KPR	K ₃ (Fe[CN] ₆)-N ₂ OH
Cr-Si	KPR	
Ta	KPR	HNO ₃ -HF
Ag	KTFR	Fe(NO ₃) ₃

K. Beam Leaded Silicon on Sapphire MOS

Silicon on sapphire promises to be a fast, closely packed, and radiation-resistant technology. In order to take advantage of these potentialities in today's complex systems, beam leading of the chips is essential. Because of the difficulty of separating sapphire into chips, a straightforward application of the recently developed MOS beam leading method is not possible.

The refractory nature of the sapphire precludes any back etch separation. At present, industry uses modified scribing techniques to separate sapphire. This is done either by diamond scribing or laser scribing. If these methods are used, a standard beam lead layout would not be possible since the scribing would slice off the beams. Instead, the layout would have to employ streets as well as eliminating beam interdigitation, resulting in a prohibitive increase in chip area.

TABLE 5. PROPERTIES OF METALS EMPLOYED AS THIN FILMS

Metal	Limiting Current Density $J_1 \text{ A/cm}^2 \times 10^5$	Resistivity $\times 10^{-6} \Omega/\text{cm}$	Remarks
Silver	4.0	1.59	Poor adhesion
Copper	4.0	1.67	Poor adhesion; corrosion
Gold	7.0	2.35	Silicon eutectic 370° C, poor adhesion
Aluminum	0.5	2.65	Silicon Eutectic 577° C, Electromigration
Aluminum + Copper	2.0		
Magnesium		4.45	Extremely reactive
Rhodium		4.51	Poor adhesion
Iridium		5.3	Poor adhesion
Tungsten	20.0	5.6	Difficult etching
Molybdenum	10.0	5.7	Corrosion susceptibility
Platinum		9.8	Poor adhesion
Titanium		55	

To combine the beam lead and silicon on sapphire technologies requires a modification of both these technologies. One may deposit a material on the sapphire in the beam lead areas (excluding the anchor pads) before the beam lead metal is deposited. This material must meet two requirements:

1. It must be capable of being etched off before scribing and after the rest of the processing is done.
2. It must stand up to the rigors of processing.

After this material has been deposited and the normal beam lead processing is complete, the beams are exposed and this undercover material is etched off leaving the ends of the beams free from connection to the substrate. The wafer can then be scribed in the normal way and interdigitation is permissible.

The undercover material to be employed will depend on the particular SOS process being employed and the process point at which it is put down. Some possibilities are silicon, SiO_2 , Si_3N_4 , Al_2O_3 and photoresist. All processes have not been worked out at the present for producing beam lead MOS division sapphire. However, within a few months a great deal of progress is expected by industry.

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APPROVAL

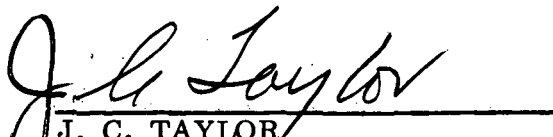
MONOLITHIC MICROCIRCUIT TECHNIQUES AND PROCESSES

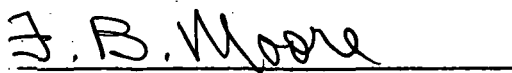
By Bobby W. Kennedy

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This document has also been reviewed and approved for technical accuracy.


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